THE APPLICATION OF PHOTOCONDUCTIVE SWITCHES IN AC CIRCUIT PROTECTION

By

CHRISTOS P. TRIAROS

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To My Father

ACKNOWLEDGMENTS

I would like to thank my family for their support and encouragement during this work. I am very grateful to my advisor, Dr. Dennis P. Carroll, for his guidance and support in completing this work. I extend a special thanks to Dr. F. Lindholm and Dr. A. Neugroschel for helpful discussions. I also thank Dr. G. Bosman, Dr. A. Domijan, and Dr. A. Varma for serving on my supervisory committee.

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LIST OF SYMBOLS

A_{pce}	PCE area for current conduction
A_{sink}	Heat sink area for thermal conduction
C_{Au}	Empirical constant used to calculate the Auger recombination lifetime
C_e	Empirical constant used to calculate the PCE saturation current
C_t^{pce}	Thermal capacitance of PCE
C_t^{sink}	Thermal capacitance of heat sink
c	Speed of light (2.998×10^8 m/sec)
c_p^{pce}	Specific heat of PCE material
c_p^{sink}	Specific heat of heat sink material
D_n	Electron diffusion coefficient
D_p	Hole diffusion coefficient
d_{unit}	Depth of one PCE unit
E	Electric field (also symbol for energy)
E_g	Energy bandgap
$E_g(0)$	Energy bandgap at 0 K
E_{max}	Maximum hold-off voltage per unit length
f	Frequency of source voltage
g	Free carrier generation rate
h	Planck's constant (6.63×10^{-34} J-sec)
h_b	Percentage of bulk optical power that is converted to heat

h_c	Convection coefficient
h_j	Percentage of junction optical power that is converted to heat
I_{br}	Breaker current
I_{pce}	PCE current
I^{off}_{pce}	PCE current under dark conditions
I^{sat}_{pce}	PCE on-state saturation current
J_n	Electron current density
J_p	Hole current density
k	Boltzmann's constant (1.38×10^{-23} J/K)
k_{pce}	Thermal conductivity of PCE material
k_{sink}	Thermal conductivity of heat sink material
L_a	Ambipolar diffusion length
L_{pce}	Electrical length of PCE
L_s	System inductance
L_{sink}	Length of heat sink
m^*_n	Electron density of states effective mass
m^*_p	Hole density of states effective mass
N^-_A	Ionized acceptor concentration
N^+_D	Ionized donor concentration
N_a	Acceptor concentration
N_c	Effective density of states in the conduction band
N_{ref}	Empirical constant used in electron mobility calculations
N_{units}	Number of units constituting one PCE
N_v	Effective density of states in the valence band
n	Free electron concentration

n_i	Intrinsic carrier concentration
n_o	Equilibrium electron concentration
n_T	Electron concentration on trap level
P_{gen}	Heat generated in PCE
P^b_{opt}	Bulk optical power
P^j_{opt}	Junction optical power
P_{ref}	Empirical constant used in hole mobility calculations
p	Free hole concentration
p_o	Equilibrium hole concentration
q	Electronic charge ($1.6x10^{-19}$ C)
R_{load}	Load resistance
R_n	Electron recombination rate
R_p	Hole recombination rate
R_{pce}	PCE resistance
R^{off}_{pce}	PCE resistance under dark conditions
R^{on}_{pce}	PCE resistance under illuminated conditions
R_s	System resistance
R_t^{cnv}	Thermal resistance between heat sink and cooling liquid
R_t^{pce}	Thermal resistance of PCE
R_t^{sink}	Thermal resistance of heat sink
R_{test}	Test resistor for experiment current measurements
T_{amb}	Ambient temperature
T_{pce}	PCE temperature
T^{max}_{pce}	Worst case temperature rise in PCE
T_{sink}	Heat sink temperature

t	Time
t_f	Time at which a fault occurs
V_i	Electrostatic potential
V_n	Electron quasi-Fermi potential
V_p	Hole quasi-Fermi potential
V_{pce}	Voltage across PCE
V^{off}_{pce}	Voltage across PCE under dark conditions
V^{sat}_{pce}	Minimum on-state voltage required across PCE to induce current saturation
V_s	Instantaneous value of source voltage
V_s^{rms}	RMS value of source voltage
V_{th}	Thermal voltage
w	Width of one PCE unit
ΔI^{sat}_{pce}	Increase in PCE saturation current due to junction optical light
Δn	Excess optically generated electron (hole) carrier concentration
α	Empirical constant used in energy bandgap calculations
β	Empirical constant used in energy bandgap calculations
γ	Empirical constant used in electron mobility calculations
δ	Empirical constant used in hole mobility calculations
δ_n	Excess electron (hole) carrier concentration during transient conditions
ϵ_s	Permittivity
η	Quantum efficiency
λ	Wavelength of optical source
μ_n	Electron mobility
μ^n_{max}	Maximum electron mobility
μ^p_{max}	Maximum hole mobility

μ^{n}_{min}	Minimum electron mobility
μ^{p}_{min}	Minimum hole mobility
μ_p	Hole mobility
ρ_{pce}	Density of PCE material
ρ_{sink}	Density of heat sink material
σ	Total electron and hole conductivity
τ	Carrier recombination lifetime
τ_{Au}	Auger recombination lifetime
τ_{SRH}	Shockley-Read-Hall recombination lifetime
ϕ	Incident amount of photons per unit time

Abstract of Dissertation Presented to the Graduate School
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CHRISTOS P. TRIAROS

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Major Department: Electrical Engineering

This study investigates the feasibility of the PCE (photoconductive circuit element) for protective switching applications in AC (alternating current) power transmission and distribution circuits. Designs using both the all-solid-state and hybrid arrangements illustrate several potential advantages over conventional protective devices, which include increased speed of operation, improved precision in interruption point, more compact designs, and greater overall reliability. Electrical, optical, and thermal models are developed for the PCE and are incorporated into a power system simulator which evaluates PCE performance during steady-state and transient operation. Simulation results at the substation, residential, and transmission levels demonstrate the feasibility of the PCE as an interruptor, especially at the higher substation and transmission levels. In addition to theoretical designs and simulations, low power prototype PCE-based breakers are fabricated and tested for proof of concept. Experimental tests exhibit the capability of the PCE to hold off large voltages, and interrupt large currents with precision and at high speeds. Furthermore, experimental results, as well as results from the numerical simulator PC-1D, are used to validate device models and confirm theoretical design results.

CHAPTER 1
INTRODUCTION

The photoconductive switch, often referred to as a photoconductive circuit element or PCE [1], may have great potential for power system applications. This study investigates the feasibility of photoconductive switches in AC circuit protection. Electrical, optical, and thermal models are developed for the PCE and are used in power system simulation studies in order to design and test PCE-based breakers. This work includes designs of all-solid-state as well as hybrid PCE-based breakers at the substation, residential, and transmission levels. It appears from these designs that the PCE may indeed have a future in circuit protection, especially at the higher system levels. Fabrication and testing of low power prototype PCE-based breakers is also part of this study. Experimental results validate theoretical expectations regarding the operation of the PCE.

1.1 Background

A large class of switching applications in the electric utility industry involves the use of mechanical switches to interrupt or limit currents in power circuits [2]. There are numerous types of breakers for both AC and DC (direct current) circuits. These breakers vary in size, principle of operation, interrupting capacity, voltage rating, etc. However, they all have several undesirable properties in common. They all are relatively slow; they are unpredictable as to precisely when they will open or close; and their interrupting capacity is limited by complex arc phenomena. The PCE appears to be an attractive

alternative or supplement to mechanical switchgear that could eliminate or minimize these undesirable features.

The PCE consists basically of semi-insulating semiconductor material, which can be made highly conductive through applying laser or other optical excitation that contains photon energy exceeding the semiconductor energy gap. The PCE can be turned on and off very rapidly [3], will conduct large currents, and will hold off very high voltages, yet can be made relatively compact. It is also a bilateral device, which is an advantage over other semiconductor switches for AC applications, and the voltage and current rating of a single unit can be easily scaled to meet the application. In principle, it is possible in a single device to switch high voltages (up to megavolts at 100 kV per cm length) and high currents (up to megamperes at 20 kA per cm width) with more precision and higher efficiency than with any other technology [4]. This switch can be designed to close faster, with less inductance, and less relative jitter than is possible with other technologies. Thus components of circuit interruptors can be made simpler, more efficient, and more compact. The large specific heat and the excellent thermal conductivity of photoconductive materials make the technology applicable to many high-power applications. Furthermore, operation of PCE switches at cryogenic temperatures can improve the optical absorption depth, carrier mobility, and mechanical properties of the device material [5]. In spite of its apparent advantages as a power switch, the PCE as yet is relatively unexplored for power system applications.

1.2 Objective

The principal objective of this study is to investigate the feasibility of the PCE for protective switching applications in AC power transmission and distribution circuits. To achieve this goal, it is planned to develop electrical, thermal, and optical models that

accurately describe the behavior of the PCE under both steady-state dark and illuminated conditions, as well as during transient operation. These PCE models will aid in the design of PCE-based breakers. The performance of these designs will be evaluated with the help of equivalent circuit calculations and by the use of digital computer simulations. Performance parameters will include: circuit interruption time, blocking voltages, interruption capacity, device losses, light source requirements, heat dissipation, and cooling methods. Furthermore, low power prototype PCE-based breakers will be fabricated and tested for proof of concept.

Chapter 2 describes the modeling of the PCE. The first section of this chapter presents the semiconductor equations that govern the physical behavior of the PCE. These equations are incorporated into the one-dimensional device simulator PC-1D [6], which is used to numerically model the current versus voltage characteristic of the PCE. The second section gives a description of the electrical models which predict the current versus voltage characteristic of the PCE during both steady-state and transient operation. The third section presents the optical models which are used to calculate the optical power required by the PCE in order to conduct the desired steady-state load current. The last section of Chapter 2 describes the thermal models which predict the temperature of the PCE during both steady-state and transient operation.

Chapter 3 evaluates the performance of PCE-based breakers during both steady-state and transient operation. The PCE is evaluated in both the all-solid-state approach and the hybrid approach. The first section of this chapter describes the power system models being utilized to test the PCE. The second section describes the power system simulator which incorporates the system and device models to numerically evaluate PCE performance. The third section presents breaker designs and simulation results for various applications. These applications include breakers operating at the substation

level, the residential level, and the transmission level. The last section of Chapter 3 compares the PCE to various GTO (Gate-Turn-Off) thyristors.

Chapter 4 describes the fabrication process and testing of low power prototype PCE-based breakers. The first section of this chapter presents a qualitative description of the fabrication process which was performed by Leslie Roberts [7] at the University of Florida's Micro Electronics Laboratories. The second section presents experimental test results for the PCE-based laboratory breakers. These results show PCE performance during both steady-state and transient operation.

CHAPTER 2
MODELING OF THE PCE

This chapter describes the modeling of the photoconductive circuit element. The first section presents the semiconductor equations that govern the physical behavior of the PCE. These equations are incorporated into the one-dimensional device simulator PC-1D [6], which is used to numerically model the current versus voltage characteristic of the PCE. The second section gives a description of the electrical models which predict the current versus voltage characteristic of the PCE during both steady-state and transient operation. The third section presents the optical models which are used to calculate the optical power required by the PCE in order to conduct the desired steady-state load current. The last section of this chapter describes the thermal models which predict the temperature of the PCE during both steady-state and transient operation.

2.1 Device Physics

Figure 2.1 shows a typical PCE which consists of an intrinsic photoconductive material, and metal/heavily doped regions which aid in obtaining ohmic contacts to the switch. An optical source is used to increase the conductivity of the PCE by generating electron-hole pairs in the bulk of the material. This section ascertains how the metal/heavily doped regions (contacts) influence the carrier profiles, the electric field profile, and the current versus voltage characteristic.

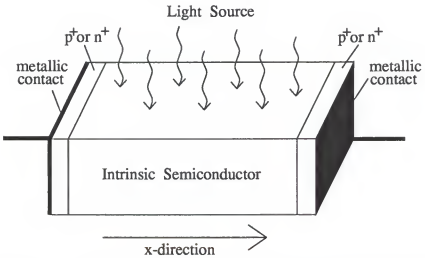

Figure 2.1. A typical photoconductive circuit element consisting of an intrinsic photoconductive material and metal/heavily doped regions.

2.1.1 The Governing Semiconductor Equations

Photogeneration, recombination, trapping, drift, and diffusion [8] are the main physical processes governing electrons and holes in a photoconductor. The system of governing equations for these processes consists of the electron and hole transport equations, the electron and hole continuity equations, Poisson's equation, and the kinetic rate equation. The one-dimensional time-dependent form of these equations is presented here.

The electron and hole transport equations are written as

$$J_n(x,t) = q\mu_n(x,t)n(x,t)E(x,t) + qD_n(x,t)\frac{\partial n(x,t)}{\partial x} \qquad (2.1\text{–}1)$$

and

$$J_p(x,t) = q\mu_p(x,t)p(x,t)E(x,t) - qD_p(x,t)\frac{\partial p(x,t)}{\partial x} \qquad (2.1\text{–}2)$$

These equations define the electron and hole current densities in terms of a drift component and a diffusion component. The drift component, which arises from carriers moving under the influence of an electric field, is proportional to the mobility, carrier

concentration, and electric field. The diffusion component, which arises from carriers moving due to a carrier gradient, is proportional to the diffusivity, and the positional rate of change of carrier concentration. The carrier concentrations may further be related to the quasi-Fermi and electrostatic potentials by the following expressions:

$$n(x,t) = n_i \exp\left(\frac{V_i(x,t) - V_n(x,t)}{V_{th}}\right) \tag{2.1–3}$$

and

$$p(x,t) = n_i \exp\left(\frac{V_p(x,t) - V_i(x,t)}{V_{th}}\right) \tag{2.1–4}$$

The electron and hole continuity equations are written as

$$\frac{\partial n(x,t)}{\partial t} = \frac{1}{q}\frac{\partial J_n(x,t)}{\partial x} + g(x,t) - R_n(x,t) \tag{2.1–5}$$

and

$$\frac{\partial p(x,t)}{\partial t} = -\frac{1}{q}\frac{\partial J_p(x,t)}{\partial x} + g(x,t) - R_p(x,t) \tag{2.1–6}$$

These differential equations describe the time dependent rate of change of electron and hole concentrations per unit volume. This temporal rate of change of carrier concentration is given in terms of the divergence of the current density, the per unit volume generation rate, and the per unit volume recombination rate. The first term accounts for all carriers entering and leaving the volume through drift and diffusion, the second term accounts for all carriers being generated in the volume by optical and thermal excitation, and the last term accounts for all carriers recombining in the volume by various recombination processes including Shockley-Read-Hall recombination, Auger recombination, and surface recombination.

Poisson's equation is written as

$$-\epsilon_s \frac{\partial^2 V_i(x,t)}{\partial x^2} = \epsilon_s \frac{\partial E(x,t)}{\partial x} = q\left[p(x,t) - n(x,t) + N_D^+(x,t) - N_A^-(x,t)\right] \tag{2.1–7}$$

This equation relates the electric field to the charge density. The charge density is given in terms of mobile carriers and localized (immobile) charge. The mobile carriers are electrons in the conduction band and holes in the valence band. The localized charge is introduced by impurities which emit and/or capture electrons. The term on the left of the first equality is introduced to indicate that the electric field is the negative gradient of the electrostatic potential.

The kinetic rate equation for a single trap level is written as

$$\frac{\partial n_T(x,t)}{\partial t} = R_n(x,t) - R_p(x,t) \tag{2.1–8}$$

This equation gives the temporal rate of change of the electron concentration on the trap, which is equal to the difference in the recombination rates of electrons and holes.

The six coupled differential equations just described are very complicated to use in the power system simulation studies. Therefore, a device simulator, which solves these equations, needs to be used to numerically model the PCE. From these numerical models simple analytical models may be derived for use in the power system simulation studies. Various device simulators [6] have been developed to numerically solve these equations. PC-1D is one such device simulator. The following part of this section presents the results from this device simulator which aided in developing several of the analytical models described in this chapter.

2.1.2 Numerical Simulations Using PC-1D

This part of the section numerically models the electrical and optical behavior of the PCE during its steady-state operation. Figure 2.2 shows the PCE, in its illuminated state with an applied voltage, as used by PC-1D for the numerical simulations being presented. The PCE consists of high resistivity bulk material to which ohmic contacts are formed. An ohmic contact may be formed by depositing metal on implanted or

diffused heavily doped regions [9]. In principle, an ohmic contact should have negligible resistance relative to the bulk resistance of the device [10]. In this section it is shown that this is not always the case.

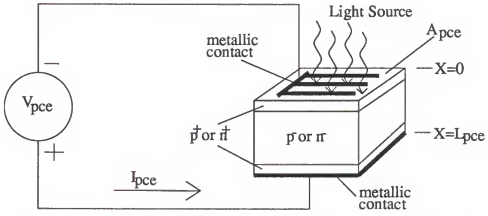

Figure 2.2. The PCE, in its illuminated state with an applied voltage, as used by PC-1D for the numerical simulations presented in this section.

High resistivity p-type semiconductors are used as bulk material for the PCEs under study. The principal reason of p-type over n-type bulk material comes from the fact that the value of hole mobility is lower than the value of electron mobility for the semiconductors under study. Therefore, other things being equal the dark resistance for the p-type material will be larger than the dark resistance of the n-type material. Two semiconductor materials are being investigated in this work, primarily Si (silicon), and in a secondary way GaAs (gallium arsenide).

The heavily doped regions which aid in obtaining ohmic contacts to the PCE also form junctions in the device. Since the PCE will be used in an AC environment there are, in principle, only two ways of forming contacts which would affect differently the operation of the device. One way is to make both heavily doped regions of the same type, that is, either p-type or n-type. This configuration always has one of the two junctions forward biased and the other reverse biased, independent of voltage polarity. The other way is to make one heavily doped region p-type and the other heavily doped

region n-type. This configuration always has both junctions either forward biased or reverse biased depending on the voltage polarity. The former of the two ways was investigated and following is a discussion on the effects of the reverse biased junction.

A Si–$p^+p^-p^+$ structure was used to numerically model the effects of the reverse biased junction on the current versus voltage characteristic, the carrier profiles, and the electric field profile. For the sign convention shown in Figure 2.2 the p^+/p^- junction is reverse biased whereas the p^-/p^+ junction is forward biased. Figure 2.3 shows a plot of current versus voltage for this device from numerical simulations using PC-1D. The current does not indefinitely increase linearly with increases in voltage, as might be expected for an ideal photoconductor, but instead saturates when the applied voltage reaches some value that depletes the reverse biased junction of carriers. Figure 2.5 shows the carrier concentration being depleted in the vicinity of the reverse biased junction for a voltage bias of 0.8 volts. The corresponding high electric field related to this depleted region is shown in Figure 2.7. This saturation effect, which limits the current carrying capabilities of the PCE, may be alleviated by generating more carriers at the reverse biased junction. One way of achieving this is to apply a second light source that would only generate carriers at the junction. Figure 2.4 shows the result of adding a second light source to the simulated case shown in Figure 2.3. The current saturation level increases from approximately 200 amps to approximately 900 amps at the expense of only 900 watts of optical power. This is due to the increase in generated carriers at the reverse biased junction, which require a higher applied voltage to deplete. Figure 2.6 shows the carrier concentration not being depleted at the reverse biased junction for the same voltage bias as in Figure 2.5. The corresponding low electric field for this case is shown in Figure 2.8.

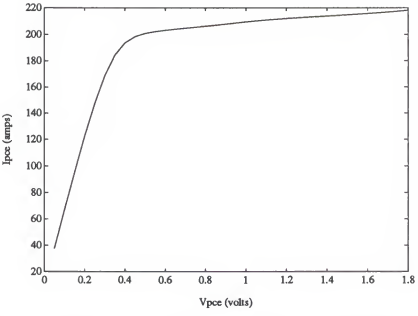

Figure 2.3. Plot of I_{pce} versus V_{pce} for a Si–$p^+p^-p^+$ structure with L_{pce}=1 mm and A_{pce}=4.5 cm^2. Other parameters include P^b_{opt}=1.8 kW @ 1.06 μm, α=10 cm^{-1}, Δn=1.37x10^{17} cm^{-3}, T_{pce}=300 K, μ_n=592 cm^2/(V.s), μ_p=207 cm^2/(V.s), and τ_{SRH}=5 μsec. The plot is from numerical simulations using PC-1D.

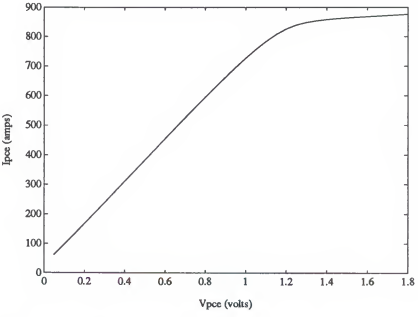

Figure 2.4. Plot of I_{pce} versus V_{pce} for same device structure and parameters as in Figure 2.3 with the addition of P^l_{opt}=900 W @ 800 nm. The plot is from numerical simulations using PC-1D.

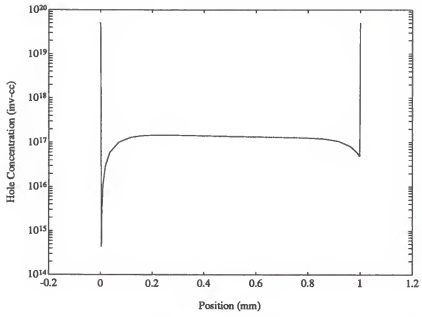

Figure 2.5. Plot of hole concentration versus position for a voltage bias of 0.8 volts. Same device structure and parameters as in Figure 2.3. The plot is from numerical simulations using PC-1D.

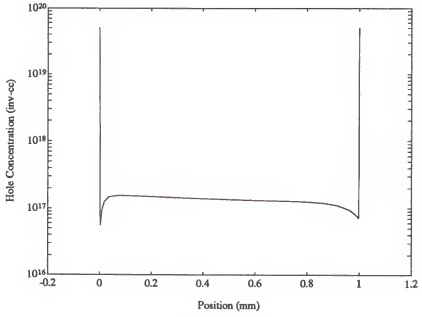

Figure 2.6. Plot of hole concentration versus position for a voltage bias of 0.8 volts. Same device structure and parameters as in Figure 2.4. The plot is from numerical simulations using PC-1D.

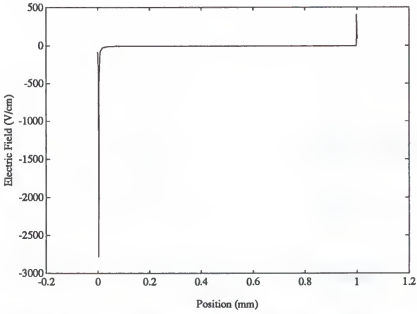

Figure 2.7. Plot of electric field versus position for a voltage bias of 0.8 volts. Same device structure and parameters as in Figure 2.3. The plot is from numerical simulations using PC-1D.

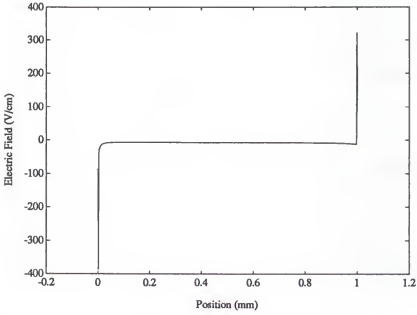

Figure 2.8. Plot of electric field versus position for a voltage bias of 0.8 volts. Same device structure and parameters as in Figure 2.4. The plot is from numerical simulations using PC-1D.

Simplified models that can predict the observed current saturation phenomenon have been developed for use in the power system simulation studies. Several simulation experiments using PC-1D have been analyzed in order to develop these simplified analog models. The results from these models are in good agreement with the device simulation results if the length of the device is several times larger than the ambipolar diffusion length. As a rule of thumb a factor of ten should be adequate. Figures 2.9, 2.11, 2.13, 2.15, and 2.17 include some of the current versus voltage plots from various simulation experiments. Figures 2.10, 2.12, 2.14, 2.16, and 2.18 show the respective saturation current versus junction light relationships. Results for Si-based devices, as well as GaAs-based devices are shown in these figures. It should be noted that because of device symmetry the current voltage relationships shown in these figures remain unchanged for negative applied voltages.

Simulation experiments using PC-1D indicate that the saturation voltage, which is defined as the applied voltage at which the current saturates, depends on several device parameters. Such parameters include device length, recombination lifetime, and optical power to the reverse biased junction. The saturation voltage changes proportionally with respect to device length and junction optical power and is inversely proportional with respect to recombination lifetime. The expression for calculating the saturation voltage is given in section 2.2.

Furthermore, these numerical experiments show that changes in the applied junction light give linear changes in the current saturation level. These experiments also suggest that this linear relationship is independent of any of the device's bulk parameters. This constant linear relationship may be observed in the slope of the saturation current versus junction light plots, which is approximately the same for the various plots of each semiconductor material.

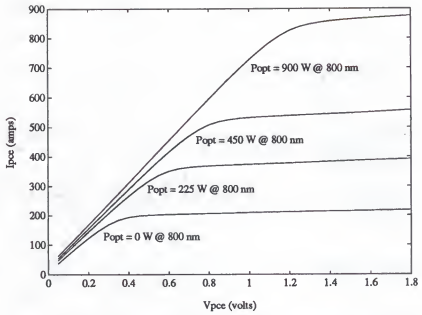

Figure 2.9. Plots of I_{pce} versus V_{pce} for a Si–$p^+p^-p^+$ structure with L_{pce}=1 mm and A_{pce}=4.5 cm^2. Other parameters include P^b_{opt}=1.8 kW @ 1.06 μm, α=10 cm^{-1}, Δn=1.36x10^{17} cm^{-3}, T_{pce}=300 K, μ_n=592 cm^2/(V.s), μ_p=207 cm^2/(V.s), and τ_{SRH}=5 μsec. The plots are from numerical simulations using PC-1D.

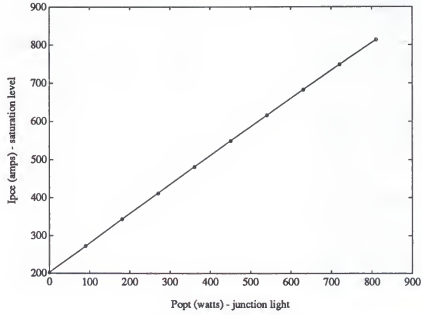

Figure 2.10. Plot of I^{sat}_{pce} versus P^i_{opt} for same device structure and parameters as in Figure 2.9. The plots are from numerical simulations using PC-1D.

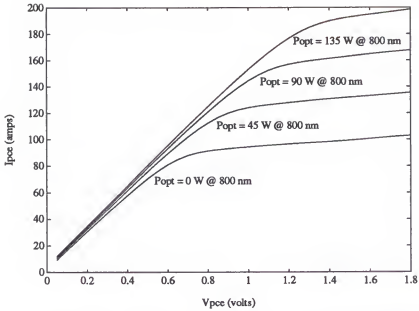

Figure 2.11. Plots of I_{pce} versus V_{pce} for a Si–$p^+p^-p^+$ structure with L_{pce}=2 mm and A_{pce}=4.5 cm^2. Other parameters include P^b_{opt}=1.8 kW @ 1.06 μm, α=5 cm^{-1}, Δn=3.8x10^{17} cm^{-3}, T_{pce}=300 K, μ_n=876 $cm^2/(V.s)$, μ_p=313 $cm^2/(V.s)$, and τ_{SRH}=2 μsec. The plots are from numerical simulations using PC-1D.

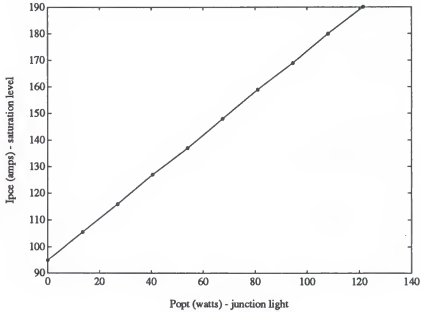

Figure 2.12. Plot of I^{sat}_{pce} versus P^j_{opt} for same device structure and parameters as in Figure 2.11. The plots are from numerical simulations using PC-1D.

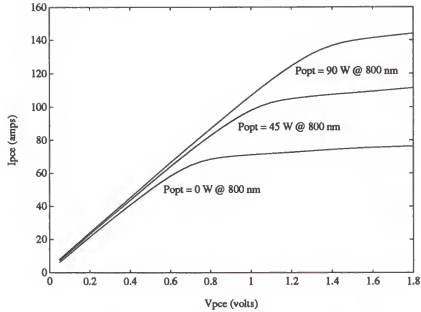

Figure 2.13. Plots of I_{pce} versus V_{pce} for a Si–$p^+p^-p^+$ structure with L_{pce}=4 mm and A_{pce}=9 cm^2. Other parameters include P^b_{opt}=1.8 kW @ 1.06 μm, α=2 cm^{-1}, Δn=2.36x10^{16} cm^{-3}, T_{pce}=300 K, μ_n=971 cm^2/(V.s), μ_p=350 cm^2/(V.s), and τ_{SRH}=5 μsec. The plots are from numerical simulations using PC-1D.

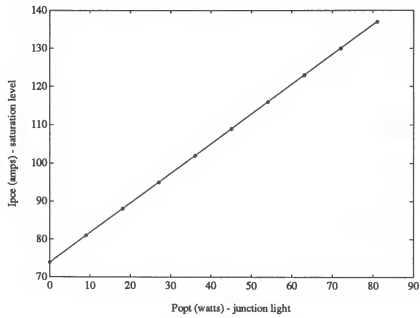

Figure 2.14. Plot of I^{sat}_{pce} versus P^j_{opt} for same device structure and parameters as in Figure 2.13. The plots are from numerical simulations using PC-1D.

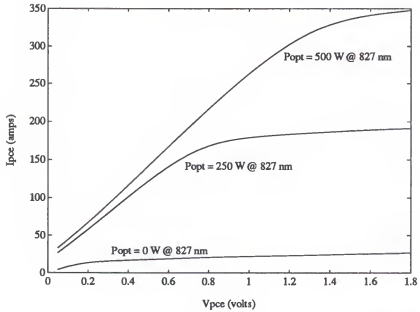

Figure 2.15. Plots of I_{pce} versus V_{pce} for a GaAs–$p^+p^-p^+$ structure with L_{pce}=0.5 mm and A_{pce}=25 cm^2. Other parameters include P^b_{opt}=500 W @ 830 nm, α=10 cm^{-1}, Δn=3.3x10^{14} cm^{-3}, T_{pce}=300 K, μ_n=8353 cm^2/(V.s), μ_p=386 cm^2/(V.s), and τ_{SRH}=100 nsec. The plots are from numerical simulations using PC-1D.

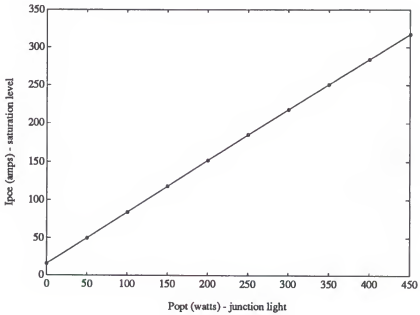

Figure 2.16. Plot of I^{sat}_{pce} versus P^j_{opt} for same device structure and parameters as in Figure 2.15. The plots are from numerical simulations using PC-1D.

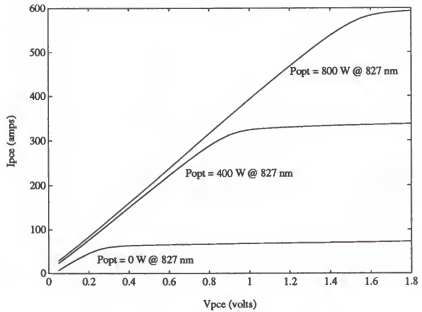

Figure 2.17. Plots of I_{pce} versus V_{pce} for a GaAs–$p^+p^-p^+$ structure with L_{pce}=2 mm and A_{pce}=4 cm^2. Other parameters include P^b_{opt}=3.2 kW @ 830 nm, α=5 cm^{-1}, Δn=1.8x10^{16} cm^{-3}, T_{pce}=300 K, μ_n=6588 cm^2/(V.s), μ_p=320 cm^2/(V.s), and τ_{SRH}=1 μsec. The plots are from numerical simulations using PC-1D.

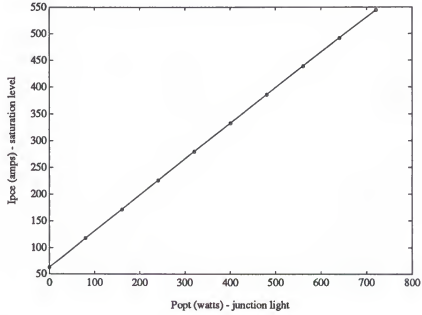

Figure 2.18. Plot of I^{sat}_{pce} versus P^j_{opt} for same device structure and parameters as in Figure 2.17. The plots are from numerical simulations using PC-1D.

2.2 Electrical Models

This section presents the electrical modeling of the PCE for steady-state as well as transient operation. The device geometry for these models is shown in Figure 2.19. The PCE consists of several units put in parallel. This is done because of limitations in the penetration depth of light which limits one of the dimensions of the device, d_{unit}, to this penetration depth. For example, the best effective penetration depth that can be achieved in silicon at room temperature is approximately one millimeter [10] when using a Neodymium-Yag laser which has a wavelength of 1.06 micrometers.

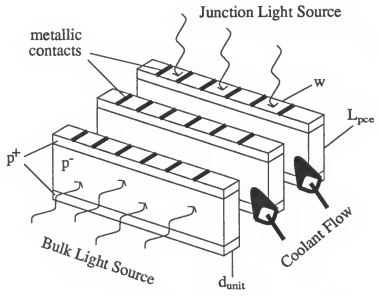

Figure 2.19. Conceptual geometry of the PCE.

The direction of the bulk light is chosen to be transverse to the direction of current. Therefore, the electrical length, L_{pce}, of the device is independent of the light penetration depth and is primarily determined by the required hold-off (blocking) voltage of the switch. The applied static electric field is limited, in principle, by the breakdown voltage of the bulk semiconductor, which for silicon is approximately [10]

$$E_{max} = \left(\frac{V_{pce}^{off}}{L_{pce}} \right) < 3(10)^5 \quad V/cm \tag{2.2–1}$$

Other mechanisms, such as surface flashover, may reduce E_{max} below the value indicated in (2.2–1). Careful engineering design, however, can alleviate the influence of such mechanisms [11].

The width, w, of each unit which depends on the total cross sectional area, A_{pce}, and the number of units, N_{units}, being used may be expressed as follows:

$$w = \frac{A_{pce}}{N_{units} d_{unit}} \tag{2.2–2}$$

The total cross sectional area depends on the imposed requirements for leakage current. The number of units is chosen so as to give a compact design.

2.2.1 Steady-State-Off Model

Under dark conditions the bulk material dominates the operation of the PCE. The applied voltage is distributed uniformly across the PCE, and under the assumption of $L_{pce} >> L_a$ there is no carrier gradient in the bulk of the device. Therefore, the electron and hole transport equations may easily be rewritten to give the following equation which treats the PCE as a resistor which behaves according to Ohm's law.

$$R_{pce} = \frac{L_{pce}}{A_{pce}\sigma} \tag{2.2–3}$$

The combined electron and hole conductivity is given by the following expression:

$$\sigma = q(\mu_n n_o + \mu_p p_o) \tag{2.2–4}$$

This nonilluminated conductivity depends strongly on temperature because of the law of mass action, $p_o n_o = n_i^2$, in which n_i depends on temperature [2]. This temperature dependence for p-type material is given by the following expressions [12]:

$$p_o = \frac{N_a + \sqrt{N_a^2 + 4n_i^2}}{2} \tag{2.2–5}$$

$$n_o = \frac{n_i^2}{p_o} \tag{2.2–6}$$

where,

$$n_i(T_{pce}) = \sqrt{N_c N_v} \exp\left(-\frac{E_g}{2kT_{pce}}\right) \tag{2.2–7}$$

and,

$$N_c = 2\left(\frac{2\pi m_n^* kT_{pce}}{h^2}\right)^{1.5} \tag{2.2–8}$$

$$N_v = 2\left(\frac{2\pi m_p^* kT_{pce}}{h^2}\right)^{1.5} \tag{2.2–9}$$

The energy bandgap shown in equation 2.2–7 is also temperature dependent. Thurmond [13] expressed this temperature dependence by the following equation:

$$E_g(T_{pce}) = E_g(0) - \frac{\alpha T_{pce}^2}{(T_{pce} + \beta)} \tag{2.2–10}$$

Furthermore, the electron and hole mobilities depend on the carrier densities. The following equations which were empirically derived by Caughey and Thomas [14] should be adequate for this work.

$$\mu_n = \frac{\mu_{max}^n - \mu_{min}^n}{1 + (N/N_{ref})^{\gamma}} + \mu_{min}^n \tag{2.2–11}$$

$$\mu_p = \frac{\mu_{max}^p - \mu_{min}^p}{1 + (P/P_{ref})^{\delta}} + \mu_{min}^p \tag{2.2–12}$$

The parameters μ^n_{max}, μ^n_{min}, N_{ref}, γ, μ^p_{max}, μ^p_{min}, P_{ref}, and δ, are empirical constants dependent on the type of carrier and semiconductor material. Variables N and P take on the value of electron and hole carrier densities, respectively.

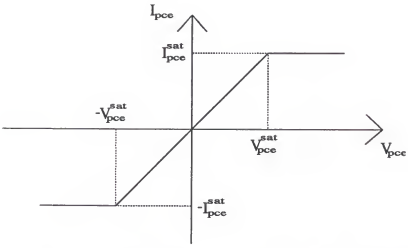

Figure 2.20. PCE current-voltage relationship under steady-state illumination.

2.2.2 Steady-State-On Model

Figure 2.20 shows the current versus voltage characteristic of the PCE for the steady-state illuminated condition. The PCE is treated as a resistor which behaves according to the following equations:

$$R_{pce} = \frac{L_{pce}}{A_{pce}\sigma} \quad for \quad -V_{pce}^{sat} \leq V_{pce} \leq V_{pce}^{sat} \tag{2.2–13}$$

$$R_{pce} = \frac{V_{pce}}{I_{pce}^{sat}} \quad for \quad V_{pce} > V_{pce}^{sat} \tag{2.2–14}$$

$$R_{pce} = \frac{V_{pce}}{-I_{pce}^{sat}} \quad for \quad V_{pce} < -V_{pce}^{sat} \tag{2.2–15}$$

Equation 2.2–13 describes the linear region of the current-voltage relationship. In this region the bulk material dominates the operation of the PCE. The applied voltage is distributed uniformly across the PCE, and under the assumption of $L_{pce} >> L_a$ there is no carrier gradient in the bulk of the device. Therefore, the electron and hole transport

equations may easily be rewritten to give equation 2.2–13, where the combined electron and hole conductivity is given by the following expression:

$$\sigma = q[(\mu_n + \mu_p)\Delta n + \mu_n n_o + \mu_p p_o] \tag{2.2–16}$$

This illuminated conductivity is dominated by the photogenerated excess carrier concentration. The temperature dependent electron and hole equilibrium carrier densities and the carrier density dependent electron and hole mobilities are given by equations 2.2–5 through 2.2–12.

Equations 2.2–14 and 2.2–15 describe the saturation regions of the current-voltage relationship. In this regions the reverse biased junctions dominate the operation of the PCE. The expressions for the saturation voltage and saturation current, which were empirically derived from the numerical simulations of the previous section, are given below:

$$V_{pce}^{sat} = \frac{L_{pce}L_a}{\mu_n \tau} + \frac{P_{opt}^{j} L_{pce}}{C_e A_{pce} \sigma} \tag{2.2–17}$$

$$I_{pce}^{sat} = \frac{V_{pce}^{sat}}{[L_{pce}/(A_{pce}\sigma)]} \tag{2.2–18}$$

The first term on the right of the equality of equation 2.2–17 determines the saturation voltage without an applied junction light. The second term determines the increase in saturation voltage when junction light is applied. Equation 2.2–18 determines the maximum current carrying capability of the PCE which is simply the saturation voltage divided by the PCE resistance in the linear region. The constant C_e gives the amount of junction light required to increase the saturation current by one ampere and is determined from the device simulation studies. The ambipolar diffusion length may be expressed in terms of carrier mobilities and recombination lifetime as follows [9]:

$$L_a = \sqrt{\frac{2\tau \mu_n \mu_p V_{th}}{\mu_n + \mu_p}} \tag{2.2–19}$$

The recombination lifetime which includes both the Shockley-Read-Hall and Auger recombination processes is given by equations 2.2–22 and 2.2–23.

Figures 2.21–2.26 show several plots of current versus voltage for various device parameters. These figures show that the results from the models given in this section are in good agreement with the results from the numerical simulations using PC-1D.

2.2.3 Turn-Off Model

The turn-off model describes the transition from the on-state conductivity to the off-state conductivity. This transition occurs when the light source is interrupted, resulting in the decay of the excess carrier concentration from its initial steady-state value to zero. The expression for this transient may be derived from the continuity equations. Under the assumption of a long device, $L_{pce} >> L_a$, which results in constant current densities in the bulk of the device, the solution to the continuity equations is given by the following expression:

$$\delta n = \Delta n \exp\left(-\frac{t}{\tau}\right) \tag{2.2–20}$$

The combined electron and hole conductivity may thus be written as

$$\sigma = q[(\mu_n + \mu_p)\delta n + \mu_n n_o + \mu_p p_o] \tag{2.2–21}$$

The recombination lifetime which accounts for both the Shockley-Read-Hall and Auger recombination processes is given by the following equation:

$$\tau = \left(\tau_{SRH}^{-1} + \tau_{Au}^{-1}\right)^{-1} \tag{2.2–22}$$

Shockley-Read-Hall recombination is usually dominant. This process involves transitions between the conduction and valence bands and deep level traps. At higher electron and hole concentrations, the impact-Auger process starts to compete for dominance with the Shockley-Read-Hall mechanism. Auger recombination utilizes a third mobile particle,

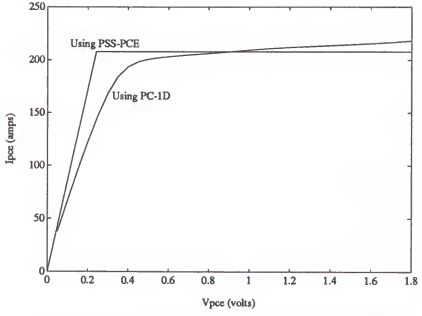

Figure 2.21. Comparison of I_{pce} versus V_{pce} from analytical models (PSS-PCE) and numerical simulations (PC-1D) for a Si–$p^+p^-p^+$ structure with L_{pce}=1 mm and A_{pce}=4.5 cm^2. Other parameters include P^b_{opt}=1.8 kW @ 1.06 μm, α=10 cm^{-1}, Δn=1.36x10^{17} cm^{-3}, T_{pce}=300 K, μ_n=592 cm^2/(V.s), μ_p=207 cm^2/(V.s), and τ_{SRH}=5 μsec.

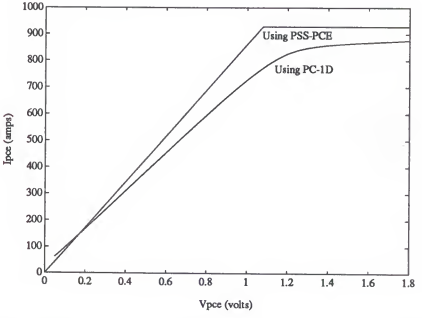

Figure 2.22. Comparison of I_{pce} versus V_{pce} from analytical models (PSS-PCE) and numerical simulations (PC-1D) for same device structure and parameters as in Figure 2.21 with the addition of P^j_{opt}=900 W @ 800 nm.

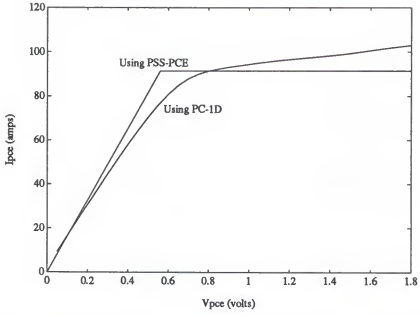

Figure 2.23. Comparison of I_{pce} versus V_{pce} from analytical models (PSS-PCE) and numerical simulations (PC-1D) for a Si–$p^+p^-p^+$ structure with L_{pce}=2 mm and A_{pce}=4.5 cm^2. Other parameters include P^b_{opt}=1.8 kW @ 1.06 μm, α=5 cm^{-1}, Δn=3.8x10^{17} cm^{-3}, T_{pce}=300 K, μ_n=876 cm^2/(V.s), μ_p=313 cm^2/(V.s), and τ_{SRH}=2 μsec.

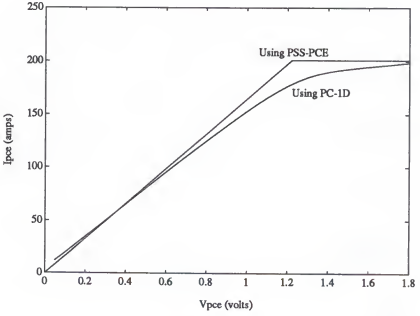

Figure 2.24. Comparison of I_{pce} versus V_{pce} from analytical models (PSS-PCE) and numerical simulations (PC-1D) for same device structure and parameters as in Figure 2.23 with the addition of P^j_{opt}=135 W @ 800 nm.

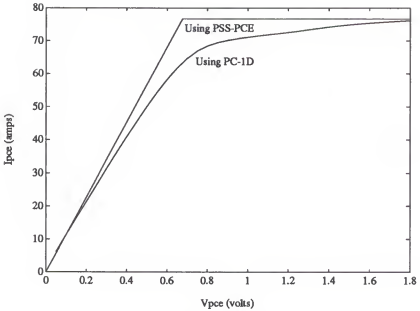

Figure 2.25. Comparison of I_{pce} versus V_{pce} from analytical models (PSS-PCE) and numerical simulations (PC-1D) for a Si–$p^+p^-p^+$ structure with L_{pce}=4 mm and A_{pce}=9 cm^2. Other parameters include P^b_{opt}=1.8 kW @ 1.06 μm, α=2 cm^{-1}, Δn=2.36x10^{16} cm^{-3}, T_{pce}=300 K, μ_n=971 cm^2/(V.s), μ_p=350 cm^2/(V.s), and τ_{SRH}=5 μsec.

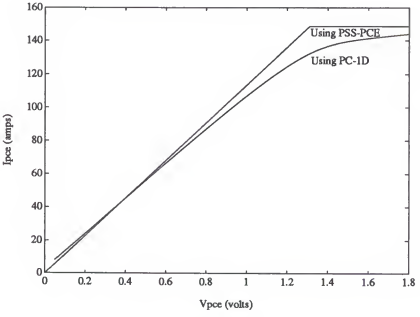

Figure 2.26. Comparison of I_{pce} versus V_{pce} from analytical models (PSS-PCE) and numerical simulations (PC-1D) for same device structure and parameters as in Figure 2.25 with the addition of P^l_{opt}=90 W @ 800 nm.

rather than phonons, to conserve energy. Thus the Auger recombination lifetime may be expressed as [15]

$$\tau_{Au} = \frac{1}{C_{Au}\Delta n^2} \tag{2.2–23}$$

2.2.4 Turn-On Model

The turn-on model describes the transition from the off-state conductivity to the on-state conductivity. This transition occurs when light is shined on the device resulting in the increase of the excess carrier concentration from its initial zero value to its final steady-state value. This transient may be expressed by the following equation:

$$\delta n = \Delta n\left[1 - \exp\left(-\frac{t}{\tau}\right)\right] \tag{2.2–24}$$

The derivation of this equation follows similar arguments to the derivation of the turn-off model. Furthermore, the total conductivity and the recombination lifetime are expressed by equations 2.2–21 and 2.2–22, respectively.

2.3 Optical Models

This section describes the optical models which are used to calculate the optical power required by the PCE in order to conduct the desired steady-state load current. Two models are required for this purpose, a bulk optical model which controls the PCE's illuminated conductivity, and a junction optical model which controls the PCE's maximum current-carrying capability.

2.3.1 Bulk Optical Model

The bulk optical model is used to calculate the optical power necessary to uniformly generate, in the bulk of the material, a desired amount of excess carrier concen-

tration. The expression for this model can be derived as follows. Each photon which penetrates the surface has an energy

$$E = \frac{hc}{\lambda} \qquad J/photon \tag{2.3–1}$$

The number of photons per second is related to the bulk optical power by the relation

$$\phi = \frac{P_{opt}^{b}}{E} \qquad photons/s \tag{2.3–2}$$

The generation rate of electron-hole pairs, given some quantum efficiency, is given by

$$g = \frac{\eta\phi}{L_{pce}A_{pce}} \qquad EHP/cm^3.s \tag{2.3–3}$$

From the continuity equations the steady-state generation rate may also be expressed as

$$g = \frac{\Delta n}{\tau} \tag{2.3–4}$$

By combining equations 2.3–1 through 2.3–4, the bulk optical power is given by the relation

$$P_{opt}^{b} = \frac{hcL_{pce}A_{pce}\Delta n}{\eta\lambda\tau} \tag{2.3–5}$$

2.3.2 Junction Optical Model

The junction optical model is used to calculate the optical power necessary, in the vicinity of the reverse biased junction, to increase the current saturation level by some desired amount. The expression for this model, which is derived empirically from the numerical simulations of section 2.1, is given by the relation

$$P_{opt}^{J} = C_e \Delta I_{pce}^{sat} \tag{2.3–6}$$

The empirical constant C_e, which is independent of any of the device's bulk parameters, gives the amount of junction light required to increase the saturation current by one ampere. For silicon C_e=1.25 W/A, and for gallium arsenide C_e=1.45 W/A.

2.4 Thermal Models

This section presents the methodology and thermal models for cooling the PCE. Two cooling methods are described in this section — cooling by heat sinking and cooling by direct immersion. The thermal models are used in the power system simulation studies to predict the temperature of the PCE during both steady-state and transient operation. Temperature is an important parameter in the operation of the PCE especially during the turn-off period. During turn-off inadequate cooling will induce a thermal runaway in the PCE which will have the effect of an unsuccessful interruption.

2.4.1 Cooling By Heat Sinking

This cooling method involves the PCE being deposited on a heat sink and the heat sink being surrounded by a cooling liquid or gas. Figure 2.27 shows the relationship between device geometry and temperature. Heat that is generated in the device due to resistive power dissipation and/or optical power dissipation is either stored in the device or conducted out of the device and into the heat sink. In turn heat conducted into the heat sink is either stored in the heat sink or conducted toward the heat sink surfaces where it is removed by convection.

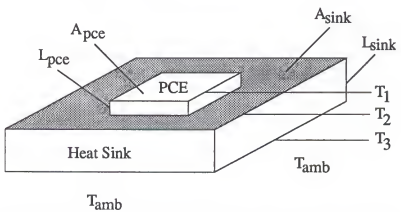

Figure 2.27. Relationship between device geometry and temperature for thermal model using cooling by heat sinking.

Under the assumptions that the top surface of the device is thermally insulated, that heat is conducted from the top surface of the device toward the bottom surface of the heat sink (x-direction), that heat is removed only at the bottom surface of the heat sink, and that a linear temperature gradient exists in the device, a one-dimensional thermal model is adequate to predict the temperature of the PCE. The differential equations describing this simplified thermal model are given below [16,17]:

$$P_{gen} = -k_{pce}A_{pce}\frac{\partial T_{pce}}{\partial x} + \rho_{pce}L_{pce}A_{pce}c_p^{pce}\frac{\partial T_{pce}}{\partial t} \tag{2.4–1}$$

$$-k_{sink}A_{sink}\frac{\partial T_{sink}}{\partial x} = h_c A_{sink}(T_3 - T_{amb}) + \rho_{sink}L_{sink}A_{sink}c_p^{sink}\frac{\partial T_{sink}}{\partial t} \tag{2.4–2}$$

Equation 2.4–1 equates the heat generated in the PCE to the sum of heat conducted out of the PCE and into the heat sink and heat stored in the PCE. Equation 2.4–2 equates the heat conducted into the heat sink to the sum of heat convected out of the heat sink and heat stored in the heat sink.

For computer simulation purposes equations 2.4–1 and 2.4–2 are discretized in the x-direction. For simplicity only three nodes are used. Figure 2.27 shows these nodes as being related to the geometries of the device and heat sink. Node 1 is taken to be the top surface of the PCE, node 2 is taken to be the interface between the PCE and the heat sink, and node 3 is taken to be the bottom of the heat sink. The discretized versions of equations 2.4–1 and 2.4–2 are given by the following expressions:

$$P_{gen} = \frac{T_1 - T_2}{R_t^{pce}} + C_t^{pce}\frac{dTpce}{dt} \tag{2.4–3}$$

$$\frac{T_2 - T_3}{R_t^{sink}} = \frac{T_3 - T_{amb}}{R_t^{cnv}} + C_t^{sink}\frac{dT_{sink}}{dt} \tag{2.4–4}$$

where,

$$P_{gen} = I_{pce}^2 R_{pce} + h_b P_{opt}^b + h_j P_{opt}^j \tag{2.4–5}$$

$$C_t^{pce} = \rho_{pce} L_{pce} A_{pce} c_p^{pce} \tag{2.4–6}$$

$$C_t^{sink} = \rho_{sink} L_{sink} A_{sink} c_p^{sink} \tag{2.4–7}$$

$$R_t^{pce} = \frac{L_{pce}}{k_{pce} A_{pce}} \tag{2.4–8}$$

$$R_t^{sink} = \frac{L_{sink}}{k_{sink} A_{sink}} \tag{2.4–9}$$

$$R_t^{cnv} = (h_c A_{sink})^{-1} \tag{2.4–10}$$

$$T_{pce} = \frac{T_1 + T_2}{2} \tag{2.4–11}$$

$$T_{sink} = \frac{T_2 + T_3}{2} \tag{2.4–12}$$

Using the relationships of equations 2.4–11 and 2.4–12 and the assumption that the heat conducted out of the PCE is equal to the heat conducted into the heat sink, equations 2.4–3 and 2.4–4 may be rewritten in terms of only T_{pce} and T_{sink} as follows:

$$P_{gen} = \frac{T_{pce} - T_{sink}}{R_{t1}} + C_t^{pce} \frac{dT_{pce}}{dt} \tag{2.4–13}$$

$$\frac{T_{pce} - Tsink}{R_{t1}} = \frac{T_{sink} - T_{amb}}{R_{t2}} + \frac{T_{sink} - T_{pce}}{R_{t3}} + C_t^{sink} \frac{dT_{sink}}{dt} \tag{2.4–14}$$

where,

$$R_{t1} = \frac{R_t^{pce} + R_t^{sink}}{2} \tag{2.4–15}$$

$$R_{t2} = R_t^{cnv} \tag{2.4–16}$$

$$R_{t3} = \frac{R_t^{cnv}\left(R_t^{pce} + R_t^{sink}\right)}{R_t^{sink}} \tag{2.4–17}$$

Figure 2.28 shows the equivalent circuit model of equations 2.4–13 and 2.4–14. Note that heat is equivalent to current in an electrical circuit, temperature is equivalent to voltage in an electrical circuit, and thermal resistances and capacitances are equivalent to resistors and capacitors in an electrical circuit, respectively.

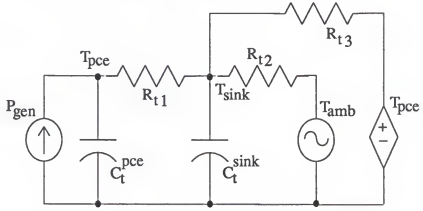

Figure 2.28. Equivalent circuit for thermal model using cooling by heat sinking.

2.4.2 Cooling By Direct Immersion

This cooling method involves the PCE being directly immersed into a cooling fluid. This technique eliminates the thermal resistance involved in heat sinking a device, and thus more heat may be extracted from the PCE. Work done by Iversen (Coriolis Corporation) and Whitaker (University of California) [18] shows a process using such a technique which results in very low junction to fluid thermal resistances and very high heat flux dissipation capabilities.

Figure 2.29 illustrates the relationship between device geometry and temperature, for one of the units of the PCE, for this cooling method. Heat that is generated in the volume of each unit is removed by forced convection at the two surfaces associated with the width and length of each unit. Assuming uniform heat generation in the volume of each unit, equal heat removal rates at the two surfaces associated with the width and length of each unit, and no heat removal at the remaining surfaces, then a one-dimensional thermal model is adequate to predict the temperature of the PCE. Furthermore, under these assumptions heat is conducted toward the heat removal surfaces via a temperature gradient within the unit. Therefore, the hottest plane related to the width and length of each unit is midpoint of the depth. The temperature at this plane is taken to be the PCE temperature.

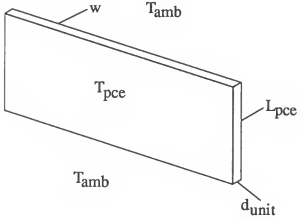

Figure 2.29. Relationship between device geometry and temperature for thermal model using cooling by direct immersion.

The differential equation describing this thermal model is given below [16,17]:

$$P_{gen} = C_t^{pce}\frac{dT_{pce}}{dt} + \frac{T_{pce} - T_{amb}}{R_t^{pce}} \tag{2.4–18}$$

where,

$$P_{gen} = \frac{I_{pce}^2 R_{pce} + h_b P_{opt}^b + h_j P_{opt}^j}{2N_{units}} \tag{2.4–19}$$

$$C_t^{pce} = \frac{\rho_{pce} c_p^{pce} w d_{unit} L_{pce}}{2} \tag{2.4–20}$$

$$R_t^{pce} = \frac{d_{unit}}{2 k_{pce} w L_{pce}} \tag{2.4–21}$$

Equation 2.4–18 equates the heat generated in half the volume of each unit to the sum of heat stored in half the volume of each unit and heat conducted out of half the volume of each unit. Figure 2.30 shows the equivalent circuit for this thermal model.

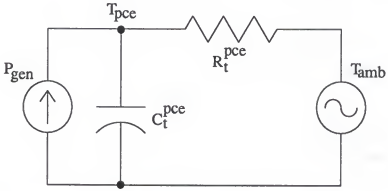

Figure 2.30. Equivalent circuit for thermal model using cooling by direct immersion.

CHAPTER 3
POWER SYSTEM SIMULATION STUDIES

This chapter evaluates the performance of PCE-based breakers during both steady-state and transient operation. The PCE is evaluated in both the all-solid-state approach and the hybrid approach. In the all-solid-state approach the breaker is composed primarily of the PCE which is used to carry the load current at all times as well as interrupt the load or fault current when required. In the hybrid approach the breaker is composed of a PCE in parallel with a mechanical switch. The mechanical switch is used to carry the load current, whereas the PCE is used to interrupt the load or fault current. The first section of this chapter describes the power system models being utilized to test the PCE. The second section describes the power system simulator which incorporates the system and device models to numerically evaluate PCE performance. The third section presents breaker designs and simulation results for various applications. These applications include breakers operating at the substation level, the residential level, and the transmission level. The last section compares the PCE to various existing GTO thyristors.

3.1 System Modeling

This section describes the power system models being utilized to test the PCE. Two types of models are being presented, the all-solid-state model and the hybrid model. Figure 3.1 shows the circuit representation of the all-solid-state model. The system is defined by a single phase source, and its relating series resistance and inductance,

connected to a purely resistive load. The breaker, which is composed of a PCE in parallel with a surge arrester, is connected between the source and the load. Furthermore, a fault switch is connected in parallel to the resistive load. Figure 3.2 shows the circuit representation of the hybrid model. The main difference between this model and the all-solid-state model is the addition of the mechanical switch in parallel to the PCE.

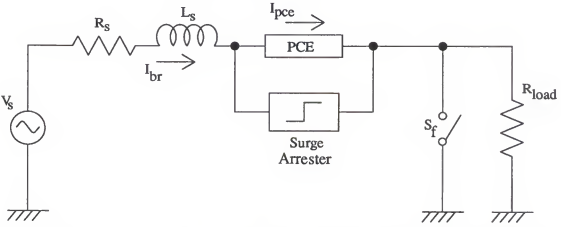

Figure 3.1. A simplified power system model for the all-solid-state approach.

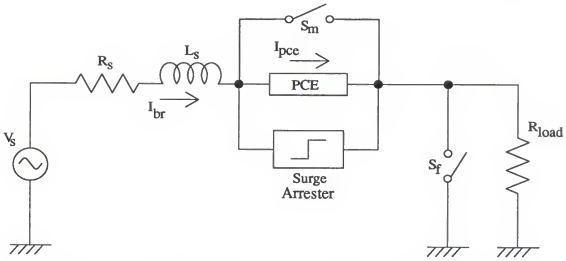

Figure 3.2. A simplified power system model for the hybrid approach.

In both these models the resistive load controls the load current. Given the system voltage the load resistance is chosen so as to give the desired load current. The fault switch is used to simulate a ground fault. When this switch closes it shorts out the

resistive load and thus generates a fault condition. The system inductance controls the amount of fault current in the system. Assuming that the inductive reactance is much larger than the combined system and breaker resistance, the fault current is equal to the system voltage divided by the inductive reactance. The system resistance is included to account for the system resistive losses.

In the all-solid-state model the breaker is defined by a PCE and a surge arrester in parallel to the PCE. In this case the PCE is required to handle the full load current as well as interrupt the flow of current when necessary. The surge arrester is included to limit the transient recovery voltage across the PCE. During an interruption the PCE experiences a high voltage buildup due to its high interrupting speed. The surge arrester helps alleviate this voltage buildup by allowing the excess current flow through it when the PCE voltage reaches the surge arrester hold-off voltage. In the simulations of this work the surge arrester hold-off voltage is chosen to be one and a half times the system voltage.

In the hybrid model the breaker is defined by a mechanical switch in parallel to a PCE and a surge arrester. In this case the load current is carried by the mechanical switch whereas the PCE is only required to handle all the necessary interruptions. In order for the PCE to interrupt, the system current has to first be commutated from the mechanical switch to the PCE. This is done by opening the mechanical switch and turning on the PCE. If commutation is successful the PCE is then turned off to complete the interruption.

The steady-state-on instantaneous breaker current may be expressed in closed form by the relation

$$I_{br}(t) = I_{on} \sin(2\pi f t - \theta_{on}) \tag{3.1–1}$$

where I_{on} and θ_{on} are given by

$$I_{on} = \frac{\sqrt{2}V_s^{rms}}{\sqrt{\left(R_{load} + R_s + R_{pce}^{on}\right)^2 + \left(2\pi f L_s\right)^2}} \tag{3.1–2}$$

$$\theta_{on} = \tan^{-1}\left(\frac{2\pi f L_s}{R_{load} + R_s + R_{pce}^{on}}\right) \tag{3.1–3}$$

for the all-solid-state model and by

$$I_{on} = \frac{\sqrt{2}V_s^{rms}}{\sqrt{\left(R_{load} + R_s\right)^2 + \left(2\pi f L_s\right)^2}} \tag{3.1–4}$$

$$\theta_{on} = \tan^{-1}\left(\frac{2\pi f L_s}{R_{load} + R_s}\right) \tag{3.1–5}$$

for the hybrid model. It should be noted that the PCE current is equal to the breaker current in the all-solid-state model, whereas, it is equal to zero in the hybrid model.

The steady-state-off instantaneous breaker current may also be expressed in closed form and is given by the relation

$$I_{br}(t) = I_{off}\sin\left(2\pi f t - \theta_{off}\right) \tag{3.1–6}$$

where I_{off} and θ_{off} are given by

$$I_{off} = \frac{\sqrt{2}V_s^{rms}}{\sqrt{\left(R_{load} + R_s + R_{pce}^{off}\right)^2 + \left(2\pi f L_s\right)^2}} \tag{3.1–7}$$

$$\theta_{off} = \tan^{-1}\left(\frac{2\pi f L_s}{R_{load} + R_s + R_{pce}^{off}}\right) \tag{3.1–8}$$

for both the all-solid-state and the hybrid models. In contrast to the steady-state-on model the PCE current is equal to the breaker current in both the all-solid-state and hybrid models.

During a fault condition in the all-solid-state model the PCE resistance changes with respect to time and thus the breaker current may not be expressed in closed form. Therefore, the describing system differential equation given by

$$\frac{dI_{br}(t)}{dt} = -\frac{R_{load} + R_s + R_{pce}(t)}{L_s} I_{br}(t) + \frac{1}{L_s} V_s(t) \tag{3.1–9}$$

is numerically solved using Runge-Kutta to determine the breaker current. On the other hand during a fault condition in the hybrid model none of the system elements is time dependent enabling a closed form solution given by the relation

$$I_{br}(t) = I_f \sin(2\pi f t - \theta_f) - \\ - \left[I_f \sin(2\pi f t_f - \theta_f) - I_{on} \sin(2\pi f t_f - \theta_{on})\right] \exp\left(\frac{t_f - t}{\tau_f}\right) \quad (3.1\text{–}10)$$

In the above equation I_f, θ_f, and τ_f are given by

$$I_f = \frac{\sqrt{2} V_s^{rms}}{\sqrt{R_s^2 + (2\pi f L_s)^2}} \quad (3.1\text{–}11)$$

$$\theta_f = \tan^{-1}\left(\frac{2\pi f L_s}{R_s}\right) \quad (3.1\text{–}12)$$

$$\tau_f = \frac{L_s}{R_s} \quad (3.1\text{–}13)$$

Furthermore, I_{on} and θ_{on} are given by equations 3.1–4 and 3.1–5, respectively.

The turn-off and turn-on processes involve transients in the PCE resistance that bar a closed form solution to the system differential equation given by 3.1–9. Therefore, during either of these processes the breaker current is calculated by numerically solving equation 3.1–9.

3.2 Power System Simulator

The system models described in the previous section are combined with the device models of Chapter 2 to develop a system simulator which tests the PCE during steady-state and transient operation. Figure 3.3 shows a block diagram illustrating the main parts of the program. The source code of the program, written in Fortran, is given in the Appendix.

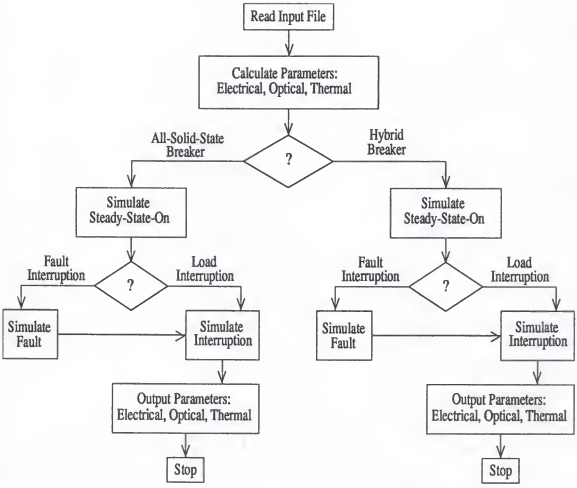

Figure 3.3. Block diagram of power system simulator.

The program first reads the input file which allows the user to specify the system level by setting the source voltage, the system resistance and inductance, and the load current. The user also specifies the type of breaker to be simulated, all-solid-state or hybrid. The user may also choose the PCE semiconductor material by assigning the material physical parameters which are required to calculate the energy bandgap, the intrinsic carrier concentration, the electron and hole mobilities, the thermal resistance, and the thermal capacitance. Furthermore, the user specifies the electrical length of the PCE, the desired leakage current, the junction optical power, as well as the temperature of the cooling environment (ambient temperature). Finally, the user selects the type of interruption to be simulated, fault interruption or load interruption.

The next step of the program is to calculate the PCE dimensions, and the steady-state electrical, optical, and thermal parameters. Using the steady-state electrical models the program calculates the device conduction area, the dark and illuminated PCE resistance, and the resistive losses under illuminated and dark conditions. Furthermore, using the optical models the program calculates the required bulk optical power to achieve the illuminated resistance, as well as the PCE saturation current. Finally, using the thermal model the program calculates the PCE temperature during both the illuminated and dark state.

Following the time independent calculations the program proceeds with the time dependent simulation. After it decides the type of breaker, all-solid-state or hybrid, to be tested it proceeds to simulate the steady-state-on condition using the system and device models for this state. These calculations continue until a fault or load interruption has to be initiated. The time for inducing a fault or a load interruption is controlled by the user. For the all-solid-state breaker a load interruption is simulated by simply turning-off the light source. The system and device turn-off models are being utilized for the simulated interruption. For the hybrid breaker an interruption is simulated by first commutating the current from the mechanical switch to the PCE, by opening the mechanical switch and turning on the PCE, and then turning off the light source. If a fault interruption is being simulated the program initiates a fault condition by closing the fault switch which eliminates the load. The program uses the system and device models for these calculations. For the hybrid breaker the fault current is allowed to build up and after several cycles an interruption is initiated near a current zero. On the other hand for the all-solid-state breaker an interruption follows the fault condition as soon as the fault is detected. The interruption process following a fault is simulated the same way a load interruption is simulated. During these time dependent calculations the program

calculates and outputs for each time step, the time, the source voltage, the breaker current, and the PCE current, voltage, resistance, power dissipation, and temperature.

Finally, the program outputs information relating to the design and experiment. This data includes, device dimensions, device dark and illuminated resistance, device dark and illuminated power dissipation, device optical requirements, and device temperature during steady-state-on and steady-state-off operation. Furthermore, information relating to the experiment includes the PCE instantaneous current when the interruption is initiated and the time interval for a successful interruption.

3.3 Designs and Results

This section presents breaker designs and simulation results for PCE-based all-solid-state and hybrid AC breakers operating at the substation level, the residential level, and the transmission level. Two semiconductor materials are used for these PCE-based breaker designs, primarily Si, and in a secondary way GaAs. Table 3.1 shows several empirical and physical parameters for Si and GaAs which are used by the power system simulator to evaluate the energy bandgap, the intrinsic carrier concentration, the electron and hole mobilities, the Auger recombination lifetime, the thermal resistance, and the thermal capacitance. These parameters were obtained from various sources which are also given in Table 3.1.

Designing the optimum PCE-based breaker for a specified application is not a trivial task. Improving one design parameter may weaken some other design parameter. Therefore, careful engineering design is required to obtain an optimum balance among the parameters of interest which include the hold-off voltage, the leakage current, the on-state maximum current, the on-state resistive losses, the on-state optical requirements, the turn-off time, and the device temperature during both steady-state and transient operation.

Table 3.1. Si and GaAs empirical and physical parameters which are used in the power system simulation studies of this work.

Empirical and Physical Parameters				
Parameters	Silicon		Gallium Arsenide	
	Value	Ref. #	Value	Ref. #
m^*_n (kg)	9.67×10^{-31}	[19]	7.74×10^{-31}	[20]
m^*_p (kg)	5.38×10^{-31}	[19]	1.00×10^{-30}	[21]
$E_g(0)$ (eV)	1.17	[13]	1.519	[13]
α (eV/K)	4.73×10^{-4}	[13]	5.405×10^{-4}	[13]
β (K)	636	[13]	204	[13]
μ^n_{max} (cm^2/V.s)	1330	[14]	8569	[6]
μ^n_{min} (cm^2/V.s)	65	[14]	961	[6]
N_{ref} (cm^{-3})	8.5×10^{16}	[14]	9.646×10^{16}	[6]
γ	0.72	[14]	0.622	[6]
μ^p_{max} (cm^2/V.s)	495	[14]	408	[6]
μ^p_{min} (cm^2/V.s)	47.7	[14]	7.5	[6]
P_{ref} (cm^{-3})	6.3×10^{16}	[14]	4.46×10^{17}	[6]
δ	0.76	[14]	0.397	[6]
k_{pce} (W/m.K)	150	[10]	46	[10]
ρ_{pce} (kg/m^3)	2328	[10]	5320	[10]
c_p^{pce} (J/kg.K)	700	[10]	350	[10]
C_{Au} (cm^6/s)	1.66×10^{-30}	[22]	4.72×10^{-30}	[23]

Furthermore, understanding how the user controlled parameters affect the calculated parameters is important since the designs are obtained on a trial and error basis using PSS-PCE. The user controlled parameters include the electrical length, the leakage current, the dark resistivity, the generated bulk carrier concentration, the SRH recombination lifetime, the junction optical power, and the ambient temperature. The calculated parameters

include the hold-off voltage, the on-state maximum current, the on-state resistive losses, the on-state bulk optical power, the turn-off time, and the device temperature during both steady-state and transient operation. The hold-off voltage is controlled by the electrical length of the device. Increasing the electrical length of the device increases the hold-off voltage. The on-state resistive losses are controlled by the electrical length, the leakage current, the generated bulk carrier concentration, and the SRH recombination lifetime. Increasing the electrical length increases the on-state resistive losses. However, the on-state resistive losses are reduced with any increases in leakage current, generated bulk carrier concentration, or SRH recombination lifetime. The turn-off time is mainly controlled by the SRH recombination lifetime. Decreasing the SRH recombination lifetime reduces the turn-off time.

The on-state maximum current (saturation level) is controlled by the electrical length, the leakage current, the SRH recombination lifetime, the generated bulk carrier concentration, and the junction optical power. The bulk optical power is controlled by the electrical length, the leakage current, the SRH recombination lifetime, and the generated bulk carrier concentration. Figure 3.4 shows the effect the electrical length has on the current saturation level as well as on the bulk optical power. Decreasing the length of the device increases the current saturation level and decreases the bulk optical power. Figure 3.5 shows the effect the leakage current has on the current saturation level as well as on the bulk optical power. Increasing the leakage current increases the current saturation level and decreases the bulk optical power. Figure 3.6 shows the effect the SRH recombination lifetime has on the current saturation level as well as on the bulk optical power. Increasing the SRH recombination lifetime increases the current saturation level and decreases the bulk optical power. Furthermore, increasing the generated carrier concentration increases both the current saturation level and the bulk

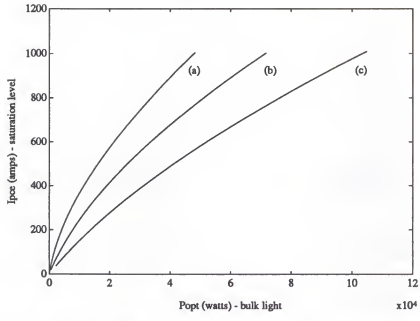

Figure 3.4. Plots of I^{sat}_{pce} versus P^{b}_{opt} for various device lengths. For all three curves I^{off}_{pce}=5 A and τ_{SRH}=5 μsec. For curve (a) L_{pce}=2 mm and A_{pce}=4.3 cm^2, for curve (b) L_{pce}=5 mm and A_{pce}=10.8 cm^2, and for curve (c) L_{pce}=10 mm and A_{pce}=21.6 cm^2. The plots are from simulations using PSS-PCE.

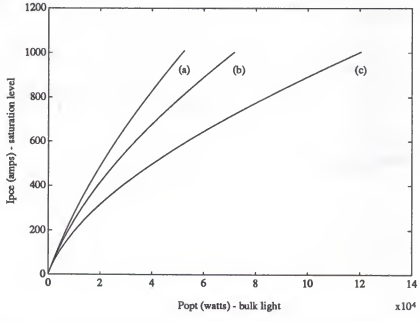

Figure 3.5. Plots of I^{sat}_{pce} versus P^{b}_{opt} for various device off-currents. For all three curves L_{pce}=5 mm and τ_{SRH}=5 μsec. For curve (a) I^{off}_{pce}=10 A and A_{pce}=21.6 cm^2, for curve (b) I^{off}_{pce}=5 A and A_{pce}=10.8 cm^2, and for curve (c) I^{off}_{pce}=2 A and A_{pce}=4.3 cm^2. The plots are from simulations using PSS-PCE.

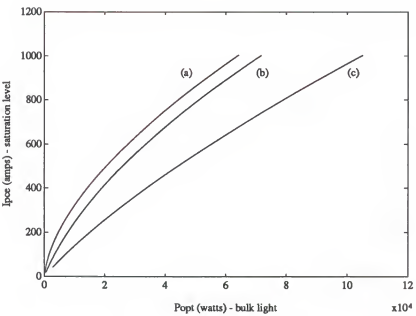

Figure 3.6. Plots of I^{sat}_{pce} versus P^{b}_{opt} for various SRH recombination lifetimes. For all three curves L_{pce}=5 mm, A_{pce}=10.8 cm^2 and I^{off}_{pce}=5 A. For curve (a) τ_{SRH}=50 μsec, for curve (b) τ_{SRH}=5 μsec, and for curve (c) τ_{SRH}=1 μsec. The plots are from simulations using PSS-PCE.

optical power. In addition, as shown in Chapter 2 the current saturation level increases linearly with increases in junction optical power. Following are some sample designs for both the all-solid-state and hybrid approaches.

3.3.1 All-Solid-State Approach

Table 3.2 shows some sample designs for the PCE-based all-solid-state AC sub-station breaker. The PCE for this application is designed to hold off the system voltage rated at 15.5 kVrms, carry a continuous load current of 600 Arms, and interrupt a fault current of 12,000 Arms. The semiconductor material used for designs 1–4 is Si, whereas GaAs is used for design 5. Design 1 is designed to have the shortest electrical length that would theoretically hold off the system voltage. This allows for a smaller device which requires less optical power and exhibits lower on-state resistive losses. Thermal

Table 3.2. Sample designs for the all-solid-state substation breaker.

All-Solid-State Substation Breaker System Voltage: 15.5 kVrms L-L Continuous Load Current: 600 Arms Fault Current: 12,000 Arms					
Design #	1	2	3	4	5
Material	Si	Si	Si	Si	GaAs
L_{pce} (mm)	2	5	5	10	5
A_{pce} (cm^2)	4.3	10.8	4.3	4.3	4.3
I^{off}_{pce} (Arms)	5	5	2	1	2.5×10^{-4}
τ_{SRH} (μsec)	2	2	4	10	1
P^{b}_{opt} (kW)	1.0	2.5	2.5	3.0	1.5
P^{i}_{opt} (kW)	1.0	1.0	1.0	1.0	1.25
R^{on}_{pce} (mΩ)	9.72	21.2	14.4	22.3	17.3
I^{sat}_{pce} (A)	848	852	862	854	876
d_{unit} (μm)	100	500	500	500	1
T_{amb} (K)	232	232	232	232	232
T^{max}_{pce} (K)	331	255	346	354	232

constraints, however, require that the depth of each unit for this design be less than the maximum allowed depth, in order to reduce the thermal resistance. Design 1 exhibits a worst case temperature rise of 99 K. The electrical length is increased in designs 2–4 in order to achieve more practical breakdown voltage to length ratios. An increase in the electrical length requires more bulk optical power and increases the on-state resistive losses. This is shown by design 2. The larger volume of design 2 allows for an increase in the depth of each unit which shows a worst case temperature rise of only

23 K. This small amount of temperature rise allows for a decrease in the conduction cross sectional area which reduces the leakage current, as well as an increase in the SRH recombination lifetime which reduces the on-state resistive losses. Design 3 shows these results along with the penalty for these improvements which is an increase of the worst case temperature rise from 23 K to 114 K. Design 4 has the longer and maybe the most practical electrical length for this application. The bulk optical power requirements are kept comparable to designs 2 and 3 by increasing the SRH recombination lifetime. This, however, reduces the speed of the device and also causes a worst case temperature rise of 124 K. Design 4 also exhibits the lowest leakage current among the Si-based designs. Note that the Si designs assume a dark resistivity of 40,000 Ω-cm at 300 K, a value limited by today's technology. In theory, intrinsic silicon at 300 K has a dark resistivity of about 800,000 Ω-cm and thus, with technological improvements, the leakage current could be reduced by about one order of magnitude. Design 5 illustrates some possible advantages in using GaAs-based PCEs. The principal advantage is a reduction in leakage current which is several orders of magnitude less than the Si designs. Another advantage might be a faster switch for comparable device dimensions, optical power requirements, and on-state resistive losses. The GaAs device is a surface device and would require much more space to accommodate as compared with a Si device of the same dimensions. This might be a disadvantage in using GaAs. If, however, compactness is not an issue, having a surface device improves device cooling.

Table 3.3 shows some sample designs for the PCE-based all-solid-state AC residential breaker. The PCE for this application is designed to hold off the system voltage rated at 480 Vrms, carry a continuous load current of 100 Arms, and interrupt a fault current of 10,000 Arms. Similar to the substation designs the semiconductor material used for designs 1–4 is Si, whereas GaAs is used for design 5. Design 1 has the smallest

Table 3.3. Sample designs for the all-solid-state residential breaker.

All-Solid-State Residential Breaker System Voltage: 480 Vrms L-L Continuous Load Current: 100 Arms Fault Current: 10,000 Arms					
Design #	1	2	3	4	5
Material	Si	Si	Si	Si	GaAs
L_{pce} (mm)	0.2	0.5	0.5	0.5	0.5
A_{pce} (cm^2)	0.56	1.4	0.69	0.69	0.54
I^{off}_{pce} (Arms)	0.2	0.2	0.1	0.1	$1.0x10^{-5}$
τ_{SRH} (μsec)	2	2	5	10	1
P^{b}_{opt} (W)	35	75	55	40	35
P^{j}_{opt} (W)	160	160	160	160	200
R^{on}_{pce} (mΩ)	3.58	8.02	6.23	5.18	7.84
I^{sat}_{pce} (A)	144	144	143	142	141
d_{unit} (μm)	200	500	500	500	1
T_{amb} (K)	273	273	273	273	273
T^{max}_{pce} (K)	325	282	314	346	273

overall dimensions and thus requires the least amount of optical power and exhibits the least amount of on-state resistive losses. Design 2 shows the effects of increasing the electrical length of design 1. These effects include an increase in optical power requirements and an increase of the on-state resistive losses. Design 3 illustrates the effects of decreasing the conduction cross sectional area and increasing the SRH recombination lifetime of design 2. These effects include a decrease in leakage current, a decrease in optical power requirements, and a decrease of the on-state resistive losses. Design

Table 3.4. Sample designs for the all-solid-state transmission breaker.

All-Solid-State Transmission Breaker System Voltage: 230 kVrms L-L Continuous Load Current: 1000 Arms Fault Current: 20,000 Arms					
Design #	1	2	3	4	5
Material	Si	Si	Si	Si	GaAs
L_{pce} (cm)	2	5	5	10	5
A_{pce} (cm^2)	5.8	14.6	7.3	5.8	5.8
I^{off}_{pce} (Arms)	10	10	5	2	$5.0x10^{-4}$
τ_{SRH} (μsec)	1	1	2	5	1
P^{b}_{opt} (kW)	30	75	70	75	35
P^{j}_{opt} (kW)	1.7	1.7	1.7	1.7	2.0
R^{on}_{pce} (mΩ)	66.4	143	97.3	170	77.8
I^{sat}_{pce} (A)	1460	1470	1490	1460	1410
d_{unit} (μm)	100	500	500	500	1
T_{amb} (K)	232	232	232	232	232
T^{max}_{pce} (K)	347	254	323	357	232

4 shows that the optical power requirements and on-state resistive losses of design 3 can be reduced even more by increasing the SRH recombination lifetime. Design 5 is a GaAs-based switch of comparable dimensions, optical power requirements, and on-state resistive losses as the Si-based devices. Similar to the substation designs the GaAs switch exhibits a reduction in leakage current which is several orders of magnitude less than the Si designs.

Table 3.4 shows some sample designs for the PCE-based all-solid-state AC transmission breaker. The PCE for this application is designed to hold off the system voltage rated at 230 kVrms, carry a continuous load current of 1000 Arms, and interrupt a fault current of 20,000 Arms. Again Si is used for designs 1–4, whereas GaAs is used for design 5. Design 1 has the smallest overall dimensions. Design 2 shows the effects of increasing the electrical length of design 1. Design 3 illustrates the effects of decreasing the conduction cross sectional area and increasing the SRH recombination lifetime of design 2. Design 4 exhibits the effects of increasing the electrical length, decreasing the conduction cross sectional area, and increasing the SRH recombination lifetime of design 3. Finally, design 5 shows the effects of designing a PCE using GaAs instead of Si.

Total power losses, including both optical and resistive, given as a percentage of total power being delivered might be one of the criteria utility companies use in deciding for or against PCE-based all-solid-state breakers. For the substation designs the total power losses range from 0.1–0.2 percent of the total per phase power being delivered. The residential designs show total power losses ranging from 0.8–1.1 percent of the total per phase power being delivered. The transmission designs exhibit total power losses ranging from 0.07–0.18 percent of the total per phase power being delivered. It appears that these percentage losses are low enough to allow consideration of the PCE-based all-solid-state breaker. The percentage losses are considerably less for the larger substation and transmission applications, thus favoring PCE-based all-solid-state breakers for applications at the higher system levels. However, this does not exclude applications at the lower system levels since the actual amount of total power losses is very small.

The designs given in Tables 3.2–3.4 were numerically tested during both steady-state and transient operation. All breakers performed successful interruptions under

any type of circumstances. Figures 3.7–3.11 show plots of various system and breaker parameters during a fault interruption at the substation level using design 4 of Table 3.2. Figure 3.7 shows a plot of the source voltage during steady-state-on, fault, and interruption. Figure 3.8 shows a plot of the breaker current, which is also the system current, during steady-state-on, fault, and interruption. In this sample case the fault occurs slightly before a current zero and results in a very large rate of change in system current. The current buildup is limited by the saturation value of the PCE which is larger than the rated continuous load current. When the system current reaches this saturation level an interruption is initiated and successfully completed as shown in Figure 3.8. Figure 3.9 shows in more detail the breaker current as well as the PCE current during this interruption. During part of the interruption the PCE current is less than the total breaker current. This is due to the high interrupting speed of the PCE which generates a large voltage buildup across the PCE. When this voltage reaches the breakdown limit of the surge arrester, it is clipped, and the excess breaker current flows through the surge arrester. Figure 3.10 illustrates the voltage buildup across the PCE during this interruption as well as the voltage clipping forced by the surge arrester. Figure 3.11 shows a plot of the PCE temperature during this interruption. The temperature rises very quickly from the on-state value of 232 K to a peak value of 295 K during interruption. The use of the surge arrester significantly aids in keeping the peak value below temperature levels that could induce a thermal runaway. The declining temperature immediately following the interruption signifies the success of the interruption. It should be noted that the waveforms of breaker and system parameters, during steady-state-on and interruption, for any system level using the all-solid-state breaker, are of the form shown in Figures 3.7–3.11.

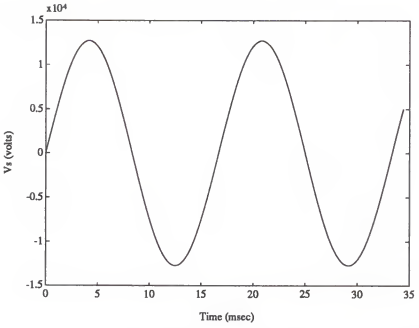

Figure 3.7. Plot of V_s during steady-state-on, fault, and interruption, for substation design #4 of Table 3.2. The plot is from numerical simulations using PSS-PCE.

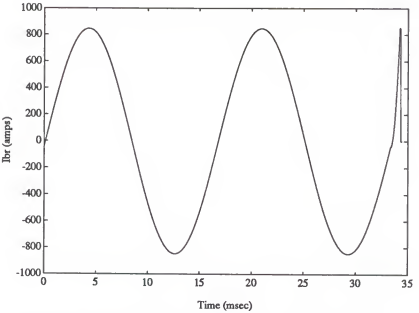

Figure 3.8. Plot of I_{br} during steady-state-on, fault, and interruption, for substation design #4 of Table 3.2. The plot is from numerical simulations using PSS-PCE.

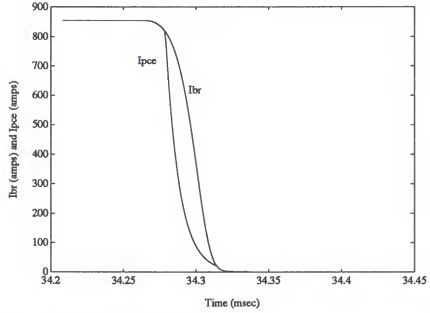

Figure 3.9. Plots of I_{br} and I_{pce} during interruption for substation design #4 of Table 3.2. The plots are from numerical simulations using PSS-PCE.

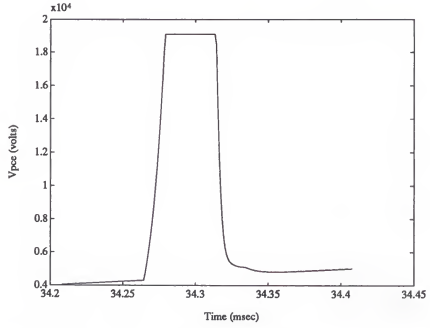

Figure 3.10. Plot of V_{pce} during interruption for substation design #4 of Table 3.2. The plot is from numerical simulations using PSS-PCE.

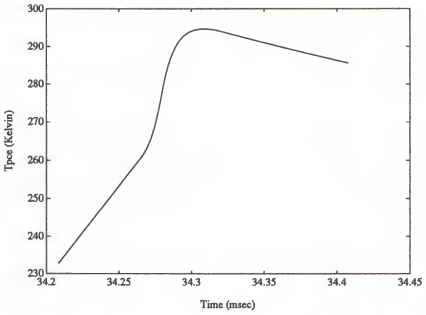

Figure 3.11. Plot of T_{pce} during interruption for substation design #4 of Table 3.2. The plot is from numerical simulations using PSS-PCE.

3.3.2 Hybrid Approach

Tables 3.5–3.7 show sample designs for PCE-based hybrid breakers operating at the substation, residential, and transmission levels. The PCE is designed to operate under illuminated conditions for 100 microseconds before and after a current zero. Under this constraint the PCE is required to handle an on-state current equivalent to the instantaneous fault current at 100 microseconds after a current zero. Furthermore, since the PCE operates under illuminated conditions for very short periods of time the on-state PCE resistance is allowed to be as large as 500 milliohms, assuming such a large value does not negate current commutation. Allowing a larger on-state PCE resistance reduces the optical power requirements. In addition, the short operating window requires fast PCE switching speeds. A SRH recombination lifetime of one microsecond provides adequate switching speed and, therefore, this value is used in all the designs.

Table 3.5. Sample designs for the hybrid substation breaker.

Hybrid Substation Breaker System Voltage: 15.5 kVrms L-L Continuous Load Current: 600 Arms Fault Current: 12,000 Arms					
Design #	1	2	3	4	5
Material	Si	Si	Si	Si	GaAs
L_{pce} (mm)	2	5	5	10	5
A_{pce} (cm^2)	0.86	2.2	1.1	2.2	1.7
I^{off}_{pce} (Arms)	1	1	0.5	0.5	$1.0x10^{-4}$
τ_{SRH} (μsec)	1	1	1	1	1
P^{b}_{opt} (W)	90	450	200	800	100
P^{j}_{opt} (W)	800	800	800	800	900
t_c (μsec)	182	187	187	187	182
R^{on}_{pce} (mΩ)	178	219	490	489	237
I^{sat}_{pce} (A)	644	647	644	647	622
d_{unit} (μm)	500	500	500	500	1
T_{amb} (K)	232	232	232	232	232
T^{max}_{pce} (K)	311	246	263	240	232

Table 3.5 shows sample designs for the PCE-based hybrid AC substation breaker. The PCE for this application is designed to hold off the system voltage rated at 15.5 kVrms and interrupt a fault current of 12,000 Arms. Silicon is used in designs 1–4 and gallium arsenide is used in design 5. Design 1 has the smallest overall dimensions and requires the least amount of optical power. Design 2 has a longer electrical length than design 1 and consequently requires more optical power. The longer length, however,

makes design 2 a better candidate for practical applications. Design 3 is an improvement of design 2 in terms of leakage current and optical power requirements. Design 4 shows the effect of increasing the electrical length of design 3 which mainly includes an increase in optical power requirements. Design 5, the GaAs-based PCE, exhibits a reduction in leakage current which is several orders of magnitude less than the Si designs. All designs exhibit low temperature rises mainly because current commutation and interruption occur near a current zero. Furthermore, because of the short conduction time the optical energy required by these designs is very small ranging from 0.178–0.325 joules.

Table 3.6 shows sample designs for the PCE-based hybrid AC residential breaker. The PCE for this application is designed to hold off the system voltage rated at 480 Vrms and interrupt a fault current of 10,000 Arms. The Si device of design 1 has the smallest overall dimensions. Design 2 is designed using a longer electrical length than design 1. Design 3 is an improvement of design 2 in terms of leakage current. Design 4 is designed using the longest electrical length. Design 5 illustrates the effects of using a GaAs-based PCE instead of a Si-based PCE. The bulk optical power in all five designs is significantly lower than the junction optical power and, therefore, increases in bulk optical power requirements due to larger overall device dimensions do not disadvantage the larger designs. Furthermore, decreases in total optical power requirements, which occur when allowing increases to the on-state PCE resistance, are insignificant and, therefore, the on-state PCE resistance in all five designs is allowed to be below 100 milliohms. The corresponding optical energy requirements for each interruption process using these designs is very small ranging from 0.14–0.16 joules. It is also worth noting that the maximum current handling capability of these designs is much larger than the continuous load current because of the large fault current and method of breaker operation.

Table 3.6. Sample designs for the hybrid residential breaker.

Hybrid Residential Breaker System Voltage: 480 Vrms L-L Continuous Load Current: 100 Arms Fault Current: 10,000 Arms					
Design #	1	2	3	4	5
Material	Si	Si	Si	Si	GaAs
L_{pce} (mm)	0.2	0.5	0.5	1.0	0.5
A_{pce} (cm^2)	0.56	1.4	0.69	1.4	2.2
I^{off}_{pce} (Arms)	0.2	0.2	0.1	0.1	$4.0x10^{-5}$
τ_{SRH} (μsec)	1	1	1	1	1
P^{b}_{opt} (W)	2	10	10	40	10
P^{j}_{opt} (W)	700	700	700	700	800
t_c (μsec)	215	215	215	215	195
R^{on}_{pce} (mΩ)	75	93	96	96	24
I^{sat}_{pce} (A)	561	562	562	563	553
d_{unit} (μm)	200	500	500	500	1
T_{amb} (K)	243	243	243	243	243
T^{max}_{pce} (K)	313	264	286	254	243

Table 3.7 shows sample designs for the PCE-based hybrid AC transmission breaker. The PCE for this application is designed to hold off the system voltage rated at 230 kVrms and interrupt a fault current of 20,000 Arms. Again Si is used in designs 1–4 and GaAs is used in design 5. Design 1 has the smallest overall dimensions and requires the least amount of optical power. Increasing the electrical length of design 1 considerably increases the optical power requirements as shown by design 2. Design 3 improves upon

Table 3.7. Sample designs for the hybrid transmission breaker.

Hybrid Transmission Breaker System Voltage: 230 kVrms L-L Continuous Load Current: 1000 Arms Fault Current: 20,000 Arms					
Design #	1	2	3	4	5
Material	Si	Si	Si	Si	GaAs
L_{pce} (cm)	2	5	5	10	5
A_{pce} (cm^2)	1.2	2.9	1.5	2.9	2.3
I^{off}_{pce} (Arms)	2	2	1	1	2.0×10^{-4}
τ_{SRH} (μsec)	1	1	1	1	1
P^{b}_{opt} (kW)	5	75	30	120	15
P^{j}_{opt} (kW)	1.4	1.4	1.4	1.4	1.5
t_c (μsec)	173	173	173	173	173
R^{on}_{pce} (mΩ)	384	196	461	461	183
I^{sat}_{pce} (A)	1140	1210	1160	1200	1050
d_{unit} (μm)	200	500	500	500	1
T_{amb} (K)	232	232	232	232	232
T^{max}_{pce} (K)	360	253	274	243	232

design 2 in terms of leakage current and optical power requirements by reducing the conduction cross sectional area and allowing a higher on-state resistance. Design 4 illustrates the effects of doubling the electrical length of design 3 which includes a quadrupling of optical power requirements. Design 5 shows the effects of using GaAs instead of Si to design the PCE-based breaker. The optical energy required per interruption process by these designs ranges from 1.3–24.3 joules.

The designs given in Tables 3.5–3.7 were numerically tested during both load and fault interruptions. The PCEs performed successfully for either of these type of interruptions. Figures 3.12–3.15 show plots of various system and breaker parameters during a fault interruption at the substation level using design 4 of Table 3.5. Figure 3.12 shows plots of the source voltage and breaker (system) current during steady-state-on and fault conditions. A line to neutral fault is initiated near a current zero resulting a large system current. The fault current is allowed to exist for several cycles before commencing the interruption process. It is worth noting the large phase shift that takes place between the source voltage and system current a few cycles following the fault occurrence. Figure 3.13 shows plots of breaker and PCE currents during current commutation and interruption. As described earlier and shown here current commutation begins within 100 microseconds prior to a current zero. After the current is transferred from the mechanical switch to the PCE, the PCE carries the fault current for approximately 200 microseconds and then proceeds with the interruption. Figure 3.14 shows a plot of the voltage across the PCE during current commutation and interruption. The voltage builds up across the PCE during the interruption and is clipped when it reaches the surge arrester breakdown voltage. Figure 3.15 shows a plot of the PCE temperature during current commutation and interruption. The temperature rise during this period is only 8 K. The declining temperature immediately following the interruption signifies the success of the interruption. The waveforms of breaker and system parameters, during steady-state-on, fault, current commutation, and interruption, for any system level using the hybrid breaker, are of the form shown in Figures 3.12–3.15.

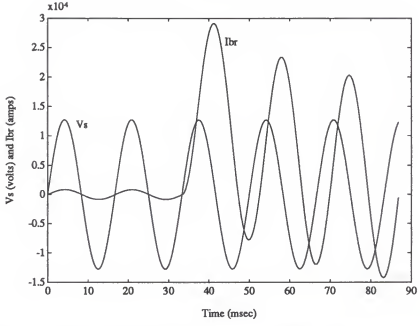

Figure 3.12. Plots of V_s and I_{br} during steady-state-on and fault for substation design #4 of Table 3.5. The plots are from numerical simulations using PSS-PCE.

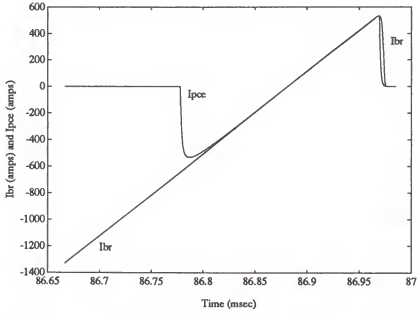

Figure 3.13. Plots of I_{br} and I_{pce} during current commutation and interruption for substation design #4 of Table 3.5. The plots are from numerical simulations using PSS-PCE.

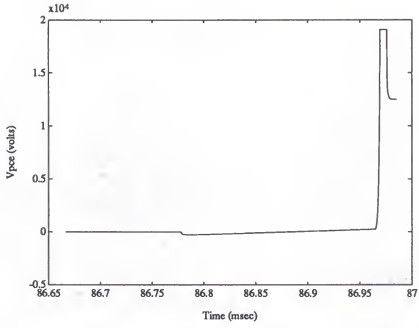

Figure 3.14. Plot of V_{pce} during current commutation and interruption for substation design #4 of Table 3.5. The plot is from numerical simulations using PSS-PCE.

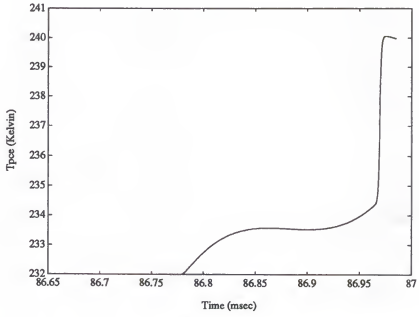

Figure 3.15. Plot of T_{pce} during current commutation and interruption for substation design #4 of Table 3.5. The plot is from numerical simulations using PSS-PCE.

3.4 Comparison of the PCE with GTO Thyristors

This section compares the PCE to conventional GTO thyristors. The PCE is a new type of semiconductor switching device which appears to have potential for power system applications. A large family of GTO thyristors, however, can already be found in use in power system applications. Therefore, a comparison between PCEs and GTO thyristors would be very informative in assessing the future of PCEs in power system applications, especially in the area of circuit protection.

As described earlier the PCE is a bilateral bulk device which can be turned on and off very rapidly, will conduct large currents, and hold off very high voltages. GTO thyristors are one-directional junction devices which can also be turned on and off very rapidly, and will conduct considerable amounts of current, but cannot hold off very large voltages. The PCE seems to have several inherent advantages over GTO thyristors. The PCE is a very simple device and, therefore, requires less fabrication processes and will probably cost less to fabricate than GTO thyristors. The PCE can be scaled to hold off any amount of voltage, whereas, GTO thyristors are limited by junction lengths to what amount of voltage they can hold off. Therefore, for very high voltage applications only one PCE is required to hold off the system voltage, whereas, many GTO thyristors in series are required to hold off the same voltage. Another advantage the PCE has over GTO thyristors is the ability to conduct current in both directions, and thus for bidirectional operation where one PCE can do the job, a combination of antiparallel GTO thyristors is required.

Table 3.8 gives a comparison between PCE-based breakers and GTO thyristor-based breakers at the substation level. Each breaker is required to hold off the system voltage when open, carry the continuous load current when closed, and interrupt a load or fault current when necessary. The table compares resistive and optical power losses

Table 3.8. Comparison of the PCE with GTO thyristors at the substation level.

System Voltage: 15.5 kVrms L-L Continuous Load Current: 600 Arms Fault Current: 12,000 Arms			
Device:	Si-PCE	GaAs-PCE	GTO Thyristors - 12 devices (Model FG1500A/70 by Powerex)
P_{el} (kW)	3.5	6.0	14.4
P_{opt} (kW)	2.0	2.75	—
I_{off} (Arms)	5	2.5×10^{-4}	0.150
t_{off} (μsec)	20	10	15

during on-state operation, leakage currents, and turn-off times. The PCE-based breakers are designs taken from Table 3.2. The Si PCE is design 1 of Table 3.2 and the GaAs PCE is design 5 of Table 3.2. The thyristor-based breaker is designed using 12 GTO thyristors which are currently available on the market. The thyristor-based breaker exhibits much higher resistive losses than both the Si and GaAs PCE-based breakers. However, the thyristor-based breaker displays no optical power losses which are inherent to the PCE-based breakers. Nevertheless, the total power losses exhibited by the PCE-based breakers are still less than the resistive losses displayed by the thyristor-based breaker. The leakage current for the Si PCE is much larger than what is allowed by the thyristors. This can be alleviated by using a GaAs-based PCE as illustrated by the results. The last parameter being compared is turn-off time. As shown by the table comparable turn-off times may be achieved using either PCEs or GTO thyristors.

In conclusion, it is safe to state that bulk photoconductive circuit elements have a promising future in power system applications, especially in the area of circuit protection.

CHAPTER 4
FABRICATION AND TESTING

This chapter describes the fabrication process and testing of low power prototype PCE-based breakers. Section one of this chapter presents a qualitative description of the fabrication process which was performed by Leslie Roberts [7] at the University of Florida's Micro Electronics Laboratories. Section two presents experimental test results for the PCE-based laboratory breakers. These results show PCE performance during both steady-state and transient operation.

4.1 Fabrication Process

This section describes the various processes involved in the fabrication of the low power PCE-based breaker. High resistivity p-type silicon wafers were used for the purposes of this work. The PCE is a bulk device and, therefore, a high resistivity semiconductor material is required in order to achieve large off to on resistance ratios. As discussed in Chapter 2 the choice of p-type material was made primarily because holes are less mobile than electrons.

Figure 4.1 shows a flowchart of the principal processes involved in the fabrication of the PCE-based breaker. The wafer to be processed goes through an initial cleaning in order to remove any surface contamination. Following this cleaning heavily doped p-type regions are formed on both wafer surfaces. These p-type regions are formed using ion implantation techniques. Boron is used for these implantations because of its well documented use. The dopant schedule is chosen to provide at least a 0.5 micron depth

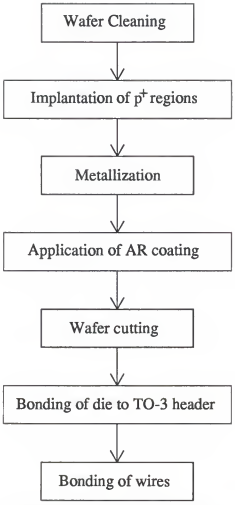

Figure 4.1. Flowchart of the principal processes involved in the fabrication of the low power PCE-based breaker.

of heavily doped region in order to achieve a low sheet resistance and, therefore, a low contact resistance [7]. Following ion implantation the wafer is cleaned again and put through an annealing process which activates the implanted dopants.

The next step in the fabrication process is to metallize both sides of the wafer. Aluminum is deposited on top of the heavily doped regions using electron beam evaporation techniques. Photolithography is then used for opening the metallization windows and for etching the metallization pattern of the top surface of each device. The final devices have a top surface aluminum coverage of approximately fifteen percent of the total surface area. Following metallization an AR (anti-reflecting) coating is applied to

the top surface of the device. This reduces the reflectivity of the top surface which results in decreases of the optical power losses.

At this point in the fabrication process the wafer is diced into individual devices. Each die is then mounted to a standard (gold plate on copper) JEDEC TO-3 header. The header allows attachment of large leads for testing purposes. It also provides a good heat sink to the PCE, and it can be attached itself to an even larger heat sink for better device cooling. The final step in the fabrication process is the bonding of wires from the two terminals of the device to the header posts using one mil diameter gold wires. The end result of this process is a Si–$p^+p^-p^+$ photoconductive circuit element. Figure 4.2 shows the top view of the fabricated PCE-based breaker. The cross sectional view is shown in Figure 4.3.

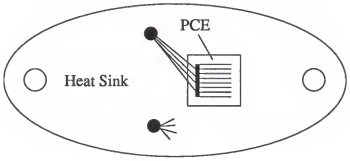

Figure 4.2. Top view of fabricated PCE-based breaker.

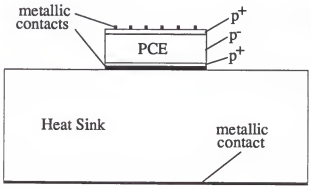

Figure 4.3. Cross-sectional view of fabricated PCE-based breaker.

The fabrication process just described does not include all the details involved in fabricating the laboratory PCE-based breaker. For a more detailed description as well as quantitative information of this process the reader is referred to Robert's work [7].

4.2 Device Testing

This section presents experimental test results for the PCE-based breakers which were fabricated at the University of Florida's Micro Electronics Laboratories. The PCE is tested under both dark and illuminated conditions as well as during both steady-state and transient operation. These tests have been very helpful in the development of the device models described in Chapter 2. Comparisons between experimental and numerical results validate theoretical expectations.

Figure 4.4 shows a schematic of the circuit being utilized to experimentally test the laboratory PCE-based breakers. The circuit consists of a 60 Hz voltage source in series with a PCE, a test resistor, and a load of light bulbs. Not part of the circuit, but required to illuminate the PCE, a 50 watt continuous wave Neodymium YAG laser is used to provide the optical power. In addition to the testing circuit and optical source several data acquisition equipment are required to record the experiments. For measuring the PCE voltage and current the LeCroy 9400A Digital Sampling Oscilloscope (DSO) is used. This scope provides a 100 megahertz sampling rate of two input channels with a storage capacity of 32,000 8–bit samples per channel. Stored data can be downloaded to a personal computer for easier processing of results. The speed and resolution of this scope is adequate for the experimental tests of this work. Optical power measurements are taken using a 50 watt power probe. Measuring the optical power being dissipated by the PCE is not a trivial task because some light is reflected by the top surface of the PCE. The absorbed optical power is estimated from measurements of the incident and reflected

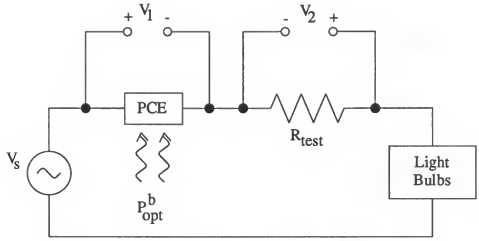

Figure 4.4. Schematic of circuit being utilized to experimentally test the laboratory PCE-based breaker.

beams. The temperature of the device is measured using a digital thermometer. This thermometer allows only steady-state temperature measurements.

The experimental test results of the laboratory PCE-based breakers are now presented. Several devices were tested during nonilluminated operation. These tests were performed using the circuit of Figure 4.4 with a source voltage of 120 volts RMS. The current versus voltage characteristic of each of the devices tested shows a nearly linear response. Furthermore, the off-state resistance of these PCEs is very close to that predicted by theory. Figure 4.5 shows the experimental nonilluminated current versus voltage characteristic of PCE #22. This plot demonstrates the ability of the PCE to hold off large voltages with small amounts of leakage current. PCE #22 has a vertical geometry similar to that shown in Figures 4.2 and 4.3 with a length of 0.5 mm and a cross-sectional area of 0.36 cm^2. The bulk material of this device is composed of p-type silicon having a resistivity of 35,000 Ω-cm. Given these device parameters the theoretical off-state resistance is indeed close to the experimental result. As the voltage increases, however, there is a drop in the off-state resistance due to inadequate device cooling. An attempt to apply larger steady-state voltages induces thermal runaway in the

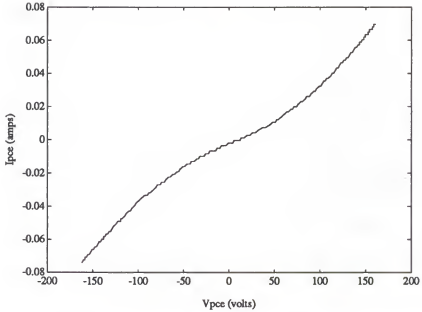

Figure 4.5. Experimental nonilluminated current versus voltage characteristic of PCE #22. Device structure as in Figures 4.2 and 4.3 with L_{pce}=0.5 mm and A_{pce}=0.36 cm^2.

device. Thermal runaway occurs when a large power dissipation in the device increases the temperature, which results in larger current. The larger current causes more power dissipation and the cycle continues until overheating results in the destruction of the device. Pulse testing [7], which reduces power dissipation, showed that the PCE was able to withstand in excess of 600 volts.

Several devices were tested during steady-state illuminated operation. The current versus voltage characteristic of each of the devices tested shows the theoretical expected linear and saturation regions. In the linear region the current is proportional to the applied voltage, whereas, in the saturation region the current is constant and independent of the applied voltage. Figure 4.6 shows the experimental illuminated current versus voltage characteristic of PCE #22 for an optical excitation of 11 watts. Figure 4.6 also shows the current versus voltage curve from numerical simulations using PC-1D. In the numerical simulations the same device dimensions as those of PCE #22 are used. Furthermore, the same optical power dissipation is used. Observation of the experimental and numerical

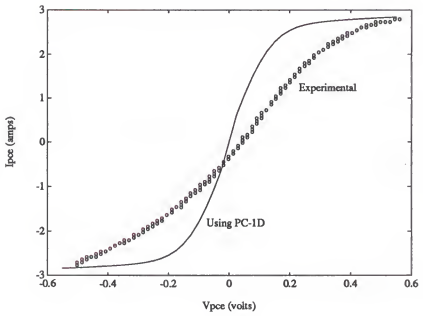

Figure 4.6. Comparison of experimental and numerical (Using PC-1D) illuminated (P^{b}_{opt}=11 W) current versus voltage characteristic for PCE #22. In the numerical simulation τ_{SRH}=4 μsec.

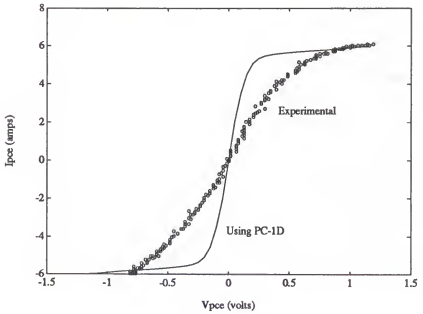

Figure 4.7. Comparison of experimental and numerical (Using PC-1D) illuminated (P^{b}_{opt}=24 W) current versus voltage characteristic for PCE #22. In the numerical simulation τ_{SRH}=4 μsec.

plots exhibited in Figure 4.6 shows identical saturation levels. This match was obtained when the SRH recombination lifetime in the numerical simulations was set to four microseconds. This result is important in that it provides a method for estimating a device's carrier lifetime.

The on-state resistance, in the linear region of both the experimental and numerical plots shown in Figure 4.6, is in the range of tenths of milliohms. The value of the experimental resistance, however, is larger than the expected numerical value. It appears this discrepancy may have two possible reasons. First, there might exist an undesirable high resistance in the contact regions due to the fabrication process. Experimental tests using some of the initial fabricated devices showed orders of magnitude larger than expected on-state resistances. Better care in fabricating the contact regions reduced drastically the on-state resistance. However, it is possible that some unwanted resistance in the contact regions of our devices still exists. A second reason for the larger experimental on-state resistance might be due to inaccuracies in the experiment itself. It is possible that high frequency noise which is generated by some of the equipment used in the experiments, and is of the order of the low voltages being measured, interferes with the accurate measurement of the device's electrical characteristics. The difference between the experimental and numerical value of the on-state resistance is not large enough to suspect a fundamental error in the analysis of photoconductive circuit elements.

Figure 4.7 shows the experimental and numerical current versus voltage plots for PCE #22 under increased optical excitation. An increase in the absorbed optical power is expected to increase the current carrying capability of the device and also reduce the on-state resistance in the linear region of the current versus voltage characteristic. These outcomes may be observed by comparing the experimental plots shown in Figures 4.6 and 4.7. Again the experimental result very closely matches the numerical result in the saturation region, whereas, some deviation exists in the linear region.

A required feature of the PCE-based breaker is the ability to interrupt large amounts of current. Several interruption experiments using the fabricated prototypes revealed very encouraging results. Several amps of current were able to be interrupted at very high speeds. Figure 4.8 shows the PCE current during and prior to a load interruption using PCE #22. As illustrated by this plot the PCE interrupts a load current, which is in excess of three amps RMS, in a matter of microseconds. It should be noted here that the switching time of the optical source is of the order of tenths of nanoseconds and thus does not degrade the measured interruption time. Figure 4.9 shows the corresponding PCE voltage for the load interruption shown in Figure 4.8. The voltage drop across the PCE is negligible prior to interruption, whereas, following the fast interruption there is a voltage build-up across the PCE equivalent to the source voltage as is expected.

Figure 4.10 shows in detail the PCE current during an experimental load interruption using PCE #22. A load interruption from a numerical simulation using PSS-PCE is also exhibited in Figure 4.10. In the numerical simulation the same device dimensions as those of PCE #22 are used. Furthermore, the same optical power dissipation is used. The SRH recombination lifetime is set to four microseconds, a value derived earlier. The testing scheme in the numerical simulation is similar to that used in the experiments. The same source voltage is applied, and the same steady-state load current is allowed to flow. The interruption in the numerical simulation is initiated at a point on the current waveform similar to that of the experimental interruption. Observation of the experimental and numerical plots exhibited in Figure 4.10 shows that the numerical result closely matches the experimental result, especially during the initial phase of the interruption. Since carrier recombination lifetime is the principal parameter affecting the numerical transient response, matching the numerical result to the experimental result via lifetime variations introduces another method for estimating a device's carrier

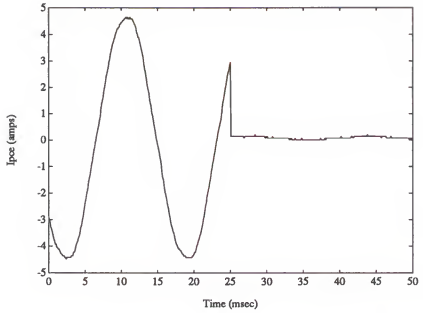

Figure 4.8. Experimental load interruption using PCE #22. P^{b}_{opt}=24 W prior to interruption. Plot shows PCE current during both steady-state and interruption.

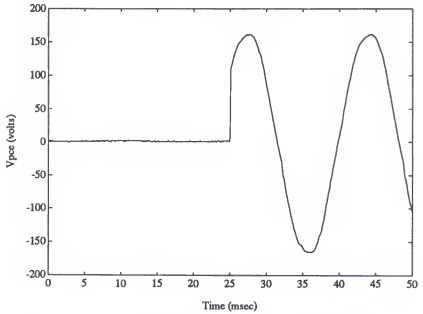

Figure 4.9. Experimental load interruption using PCE #22. Plot shows PCE voltage for same interruption as in Figure 4.8.

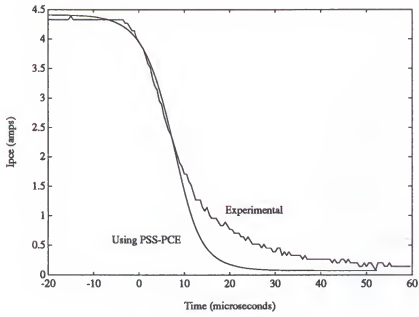

Figure 4.10. Comparison of experimental and numerical (Using PSS-PCE) load interruption using PCE #22. P^{b}_{opt}=24 W prior to interruption. In the numerical simulation τ_{SRH}=4 μsec.

recombination lifetime. The experimental result shows a larger leakage current at the tail end of the interruption process. This larger than expected leakage current is due to a significant increase in the temperature of the device during on-state operation. Better device cooling can alleviate this problem.

The experimental results described in this section are consistent with the theoretical analysis presented in Chapter 2. The tested devices exemplified the ability to hold off large voltages with low leakage currents, carry significant amount of load current with minimal resistive losses, and accurately interrupt a load current at very high speeds. Furthermore, comparisons between experimental and numerical results validate the device modeling of Chapter 2.

CHAPTER 5
CONCLUSIONS AND FUTURE RESEARCH

This study investigated the feasibility of the PCE for protective switching applications in AC power transmission and distribution circuits. Designs using both the all-solid-state and hybrid arrangements illustrate several potential advantages which include increased speed of operation, improved precision in interruption point, more compact designs, and greater overall reliability. Electrical, optical, and thermal models were developed for the PCE and were incorporated into a power system simulator which evaluates PCE performance during steady-state and transient operation. Simulation results at the substation, residential, and transmission levels show the feasibility of the PCE as an interruptor, especially at the higher substation and transmission levels if one is to consider the electrical losses involved in operating the PCE. In addition to theoretical designs and simulations, low power prototype PCE-based breakers were fabricated and tested for proof of concept. Experimental tests illustrate the ability of the PCE to interrupt significant amounts of current with precision and at high speeds. Furthermore, experimental results as well as results from the numerical simulator PC-1D, validate the device models and confirm theoretical design results.

More work, especially in the area of fabrication and testing, is probably required before the PCE could become an attractive alternative for various switching applications in the power utility industry. Fabrication and testing of devices for use at high current and voltage ratings is one possible area for future research. This task will require careful engineering design in order to achieve a robust device which could handle all

the strenuous electrical, optical, and thermal requirements of the PCE. Experimental work using two light sources, one for bulk carrier generation and one for junction carrier generation, is another area for future research. Such testing would illustrate the enormous savings in optical power requirements due to increased carrier generation in the junction areas. Fabrication of GaAs-based PCEs as an alternative to Si-based PCEs is yet another area for future research. As demonstrated by theoretical designs in this study, GaAs devices could reduce leakage currents and increase interruption speeds with comparable on-state electrical and optical losses as those exhibited by the Si devices. More theoretical work could be done in the area of device physics in order to further refine device models. For example, the transient electrical models could be refined to account for the effect of the transit time. Finally, more numerical experiments using more complex power system models could be made in order to test the PCE in a more realistic environment.

APPENDIX

SOURCE CODE FOR PSS-PCE

```
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C                    POWER SYSTEM SIMULATOR
C                            USING
C              PHOTOCONDUCTIVE CIRCUIT ELEMENTS
C
C                           (PSS-PCE)
C
C                        >>> VERSION 8 <<<
C
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Brief Description: The power system simulator (PSS) uses PCE
C                      models (electrical, thermal, and optical)
C                      to simulate load and fault interruptions.
C                      The PCE is used in both the all solid
C                      state approach as well as in the hybrid
C                      approach.
C
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   List of Variables:
C
C   A : PCE area for current conduction
C   alfe : Exponent factor in electron mobility calculations
C   alfh : Exponent factor in hole mobility calculations
C   alpha : Constant in units of eV/K used in Eg calculation
C   beta : Constant in units of K used in Eg calculation
```

```
C   c : Speed of light
C   CAu : Constant for calculating the Auger lifetime
C   Ce : Empirical constant relating Pjopt to Ipcemx
C   Cflt : Magnitude of current phasor during fault
C   cntr : Controls number of iterations
C   Con : Magnitude of current phasor during steady-state-on
C   convrg : Checks for convergence problems
C   Cp : Specific heat of semiconductor material
C   Ctpce : Thermal capacitance of PCE
C   d : Depth of PCE (same direction as light)
C   delint : Estimated interruption period (~20 X tau)
C   dt : Simulation time step (variable)
C   dtint : Actual interruption period
C   dunit : Depth of each PCE subunit
C   Ego : Bandgap at 0 degrees Kelvin
C   EgT : Bandgap of PCE material
C   f : Frequency of power source
C   F1 : Stores results of FUN
C   F2 : Same as F1
C   F3 : Same as F1
C   F4 : Same as F1
C   FUN : Calculates system current using Runge-Kutta
C   FUN1 : Calculates PCE temperature using Runge-Kutta
C   Ge1 : Stores results of FUN1
C   Ge2 : Same as Ge1
C   Ge3 : Same as Ge1
C   Ge4 : Same as Ge1
C   h : Planck's constant
C   Ibr : Breaker current in amps
C   icntr : Controls number of iterations
C   Ipce : PCE current in amps
C   Ipcemx : PCE saturation current in amps
C   Ipceof : PCE off-current in Arms
C   Ipceon : PCE on-current in Arms
C   Ipcetf : Current through PCE at tf
C   Ipceti : Current through PCE at ti
C   Ipceto : Current through PCE at to
C   k : Boltzmann's constant
C   kpce : Thermal conductivity of PCE
C   l : Length of PCE
C   La : Ambipolar diffusion length
C   lmd : Wavelength of optical source
C   Ls : System inductance
```

```
C   Mmne : Minimum electron mobility
C   Mmnh : Minimum hole mobility
C   Mmxe : Maximum electron mobility
C   Mmxh : Maximum hole mobility
C   Mn : Electron density of states effective mass
C   Mo : Electronic rest mass
C   Mp : Hole density of states effective mass
C   Mun : Mobility of electrons in PCE
C   Munoff : Mobility of electrons during off-state
C   Munon : Mobility of electrons during on-state
C   Mup : Mobility of holes in PCE
C   Mupoff : Mobility of holes during off-state
C   Mupon : Mobility of holes during on-state
C   Na : Acceptor doping concentration
C   Nc : Effective density of states in the conduction band
C   Ni : Intrinsic carrier concentration
C   Nmax : Generated carrier concentration
C   No : Hole equilibrium concentration in PCE
C   Nrfe : Reference concentration for electron mobility calc
C   Nrfh : Reference concentration for hole mobility calc
C   Numdev : Number of PCE subunits in parallel (d/dunit)
C   Nv : Effective density of states in the valence band
C   one : one = 1.0
C   phiflt : Phase of current phasor during fault
C   phion : Phase of current phasor during steady-state-on
C   pi : pi = 3.14159265
C   Pjopt : Required optical power at the junctions
C   Po : Electron equilibrium concentration in PCE
C   Pop : PCE instantaneous optical power
C   Popt : Required optical power during on-state
C   Ppce : Instantaneous power dissipation by PCE
C   Ppceof : Average power dissipation by PCE during off-state
C   Ppceon : Average power dissipation by PCE during on-state
C   q : Electronic charge magnitude
C   qe : Quantum efficiency
C   Rbr : Total breaker resistance
C   rho : Density of semiconductor material
C   Rload : System load resistance
C   Rloadi : Saves value of Rload
C   Rm : Mechanical breaker resistance
C   Rmof : Mechanical breaker resistance during off-state
C   Rmon : Mechanical breaker resistance during on-state
```

```
C   Rpce : PCE resistance
C   Rpceof : PCE resistance during off-state
C   Rpceon : PCE resistance during on-state
C   Rs : System resistance
C   Rtot : PCE bulk resistance + PCE junction resistance
C   Rtpce : PCE thermal resistance
C   six : six = 6.0
C   t : Simulation time
C   Tamb : Ambient temperature
C   tau : Recombination lifetime (includes Auger and SRH)
C   tauAu : Auger recombination lifetime
C   taufIt : Time constant for dumping after fault occurs
C   taum : Time constant for Rm on-to-off transition
C   tauSRH : SRH recombination lifetime
C   Temp : PCE temperature
C   tend : Time when each simulation process is completed
C   tendi : Time when interruption is completed
C   test1 : Choice of breaker:
C               test1=1 >>> all solid state
C               test1=2 >>> hybrid
C   test2 : Choice of simulation:
C               test2=1 >>> only steady-state calculations
C               test2=2 >>> fault simulation
C               test2=3 >>> interrupt simulation
C               test2=4 >>> fault followed by interruption
C               test2=5 >>> Popt versus Ipce calculations
C   tf : Time when fault occurs
C   ti : Time when interruption begins
C   to : Time when PCE turns on (hybrid breaker)
C   Toff : PCE temperature during off-state
C   Ton : PCE temperature during on-state
C   two : two = 2.0
C   V : Volume of PCE
C   var(i) : Variables used for intermediate calculations
C   Vpce : PCE voltage in volts
C   Vpceof : PCE off-voltage in Vrms
C   Vpceon : PCE on-voltage in Vrms
C   Vs : Source voltage in volts
C   Vsat : PCE on-voltage at which Ipce saturates
C   Vsrms : Source voltage in Vrms
C   Vstf : Source voltage at tf
C   Vsti : Source voltage at ti
```

```
C   Vsto :  Source voltage at to
C   Vth :  Thermal voltage
C   w :  Width of PCE
C   X : Vector storing t and Ibr
C   X1 :  Vector storing PCE Temp
C   Y : Vector storing intermediate steps of X
C   Y1 :  Vector storing intermediate steps of X1
C
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C                MAIN PART OF PROGRAM - CONTROL UNIT
C
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Define program variables:
C
      IMPLICIT DOUBLE PRECISION (A-Z)
      INTEGER convrg
      COMMON/blk01/Mmxe,Mmne,Nrfe,alfe,Mmxh,Mmnh,Nrfh,alfh
      COMMON/blk02/Mun,Mup/blk03/No,Po/blk04/Nmax/blk05/one
      COMMON/blk06/t/blk07/to/blk08/tau/blk09/ti
      COMMON/blk10/alpha,beta,Ego/blk11/Mn,Mp/blk12/h,k
      COMMON/blk13/Na/blk14/pi/blk15/Temp/blk16/two
      COMMON/blk17/Ctpce,Rtpce/blk18/Numdev/blk19/Tamb/blk20/Pop
      COMMON/blk21/Ppce/blk22/dt/blk23/six/blk25/f
      COMMON/blk26/Ls/blk27/Rbr/blk28/Rload/blk29/Rs/blk30/Vsrms
      COMMON/blk31/Ibr/blk33/Cflt,phiflt,tauflt
      COMMON/blk34/Con,phion/blk35/Mo/blk36/Ipceof,Ipceon
      COMMON/blk37/Cp,kpce,rho/blk38/d/blk39/dunit/blk40/l
      COMMON/blk41/Ce/blk42/delint/blk43/lmd/blk44/Pjopt/blk45/qe
      COMMON/blk46/Rmof/blk47/Rmon/blk48/taum/blk49/tauSRH
      COMMON/blk50/test1/blk51/test2/blk52/tf/blk53/Toff
      COMMON/blk54/c/blk55/V,w/blk56/A/blk57/tauAu/blk58/Ton
      COMMON/blk59/Ppceof,Ppceon,Rpceof,Rpceon,Vpceof,Vpceon
      COMMON/blk60/Rloadi/blk61/Ipcemx/blk62/Popt/blk63/q
      COMMON/blk64/convrg/blk65/Ipce/blk66/Rpce,Vpce,Vs
      COMMON/blk67/Ipcetf,Vstf/blk68/Ipceti,Vsti,tendi,dtint
      COMMON/blk69/Ipceto,Vsto/blk70/CAu
```

```
C
C   Open input and output files:
C
      OPEN (UNIT=5,FILE='Pce8.in')
      OPEN (UNIT=6,FILE='Pcedev')
      OPEN (UNIT=7,FILE='PopImx')
      OPEN (UNIT=8,FILE='Pceiv')
      OPEN (UNIT=10,FILE='Time')
C
C   Read data from input file:
C
      CALL PCEIN
C
C   Define various constants:
C
      CALL PHYCON
C
C   Check whether or not calculations of the PCE maximum
C   on-current versus optical power are desired:
C
      IF (INT(test2).NE.5) GO TO 10
C
C   Calculate and output the PCE maximum on-current versus
C   optical power:
C
      CALL IMXPOP
      GO TO 100
C
C   Calculate the PCE dimensions as well as the PCE steady-state
C   conditions:
C
   10 CALL PCEDIM
C
C   Check whether or not simulation is desired:
C
      IF (INT(test2).EQ.1) GO TO 100
C
C   Calculate and output breaker parameters during system
C   on-state:
C
      IF (INT(test1).EQ.1) THEN
        CALL PSON1
```

```
      ELSE
         CALL PSON2
      ENDIF
      IF (convrg.EQ.1) GO TO 100
C
C     Check whether or not fault simulation is desired:
C
      IF (INT(test2).NE.2.AND.INT(test2).NE.4) GO TO 20
C
C     Calculate and output breaker parameters during system
C     fault-state:
C
      IF (INT(test1).EQ.1) THEN
         CALL PSFLT1
      ELSE
         CALL PSFLT2
      ENDIF
      IF (convrg.EQ.1) GO TO 100
C
C     Check whether or not interrupt simulation is desired:
C
   20 IF (INT(test2).NE.3.AND.INT(test2).NE.4) GO TO 100
C
C     Calculate and output breaker parameters during system
C     interruption-state:
C
      IF (INT(test1).EQ.1) THEN
         CALL PSINT1
      ELSE
         CALL PSINT2
      ENDIF
C
C     Output the given and calculated information regarding
C     the PCE:
C
  100 CALL PCEDEV
C
C     Stop execution of program:
C
      STOP
      END
```

```
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine PCEIN is used to read the input file:
C
      SUBROUTINE PCEIN
      IMPLICIT DOUBLE PRECISION (A-Z)
      COMMON/blk01/Mmxe,Mmne,Nrfe,alfe,Mmxh,Mmnh,Nrfh,alfh
      COMMON/blk04/Nmax/blk06/t/blk07/to/blk09/ti
      COMMON/blk10/alpha,beta,Ego/blk11/Mn,Mp/blk13/Na/blk19/Tamb
      COMMON/blk25/f/blk26/Ls/blk29/Rs/blk30/Vsrms
      COMMON/blk36/Ipceof,Ipceon/blk37/Cp,kpce,rho/blk38/d
      COMMON/blk39/dunit/blk40/l/blk41/Ce/blk42/delint/blk43/lmd
      COMMON/blk44/Pjopt/blk45/qe/blk46/Rmof/blk47/Rmon
      COMMON/blk48/taum/blk49/tauSRH/blk50/test1/blk51/test2
      COMMON/blk52/tf/blk53/Toff/blk70/CAu
      READ (5,10) Vsrms
      READ (5,10) f
      READ (5,10) Ipceof
      READ (5,10) Ipceon
      READ (5,10) l
      READ (5,10) d
      READ (5,10) dunit
      READ (5,10) Mn
      READ (5,10) Mp
      READ (5,10) Ego
      READ (5,10) alpha
      READ (5,10) beta
      READ (5,10) Mmxe
      READ (5,10) Mmne
      READ (5,10) Nrfe
      READ (5,10) alfe
      READ (5,10) Mmxh
      READ (5,10) Mmnh
      READ (5,10) Nrfh
      READ (5,10) alfh
      READ (5,10) rho
      READ (5,10) Cp
      READ (5,10) kpce
      READ (5,10) Tamb
      READ (5,10) Toff
      READ (5,10) Na
```

```
      READ (5,10) Nmax
      READ (5,10) qe
      READ (5,10) tauSRH
      READ (5,10) CAu
      READ (5,10) lmd
      READ (5,10) Pjopt
      READ (5,10) Ce
      READ (5,10) Ls
      READ (5,10) Rs
      READ (5,10) Rmon
      READ (5,10) Rmof
      READ (5,10) taum
      READ (5,10) test1
      READ (5,10) test2
      READ (5,10) t
      READ (5,10) tf
      READ (5,10) to
      READ (5,10) ti
      READ (5,10) delint
   10 FORMAT (52X,E13.6)
      RETURN
      END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine PHYCON is used to define various constants:
C
      SUBROUTINE PHYCON
      IMPLICIT DOUBLE PRECISION (A-Z)
      COMMON/blk05/one/blk12/h,k/blk14/pi/blk16/two/blk23/six
      COMMON/blk35/Mo/blk54/c/blk63/q
      h = 0.663D-33
      c = 0.2998D+09
      q = 0.16D-18
      k = 0.138D-22
      Mo = 0.911D-30
      pi = 3.141592654
      one = 1.0
      two = 2.0
      six = 6.0
      RETURN
      END
```

```
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine IMXPOP calculates and outputs the PCE maximum
C   on-current versus optical power:
C
      SUBROUTINE IMXPOP
      IMPLICIT DOUBLE PRECISION (A-Z)
      INTEGER I
      COMMON/blk04/Nmax/blk18/Numdev/blk20/Pop
      COMMON/blk36/Ipceof,Ipceon/blk38/d/blk44/Pjopt/blk58/Ton
      COMMON/blk61/Ipcemx/blk62/Popt
      Nmaxx = 5.0D+21
      Nmax = Nmaxx
      var1 = 0.5
      var2 = 350.0
      var3 = 1000.0
      DO 20 I=3, 300
      CALL PCEDIM
      d = d*Numdev
      Ipceof = Ipceof*Numdev
      Ipceon = Ipceon*Numdev
      Popt = Popt*Numdev
      Pjopt = Pjopt*Numdev
      Pop = Popt+Pjopt
      Ipcemx = Ipcemx*Numdev
      Nmax = var1*DBLE(FLOAT(I))*Nmaxx
      WRITE (7,10) Ipcemx, Pop, Ton
   10 FORMAT (1X,3(E14.7,1X))
      IF (Ton.GT.var2) GO TO 30
      IF (Ipcemx.GT.var3) GO TO 30
   20 CONTINUE
   30 d = d/Numdev
      Ipceof = Ipceof/Numdev
      Ipceon = Ipceon/Numdev
      Popt = Popt/Numdev
      Pjopt = Pjopt/Numdev
      Ipcemx = Ipcemx/Numdev
      RETURN
      END
```

```
C*********************************************************************
C*********************************************************************
C*********************************************************************
C
C   Subroutine PCEDIM is used to calculate the PCE dimensions
C   as well as the steady-state conditions:
C
      SUBROUTINE PCEDIM
      IMPLICIT DOUBLE PRECISION (A-Z)
      COMMON/blk01/Mmxe,Mmne,Nrfe,alfe,Mmxh,Mmnh,Nrfh,alfh
      COMMON/blk04/Nmax/blk05/one/blk08/tau/blk10/alpha,beta,Ego
      COMMON/blk11/Mn,Mp/blk12/h,k/blk13/Na/blk14/pi/blk15/Temp
      COMMON/blk16/two/blk17/Ctpce,Rtpce/blk18/Numdev/blk19/Tamb
      COMMON/blk20/Pop/blk28/Rload/blk29/Rs/blk30/Vsrms/blk35/Mo
      COMMON/blk36/Ipceof,Ipceon/blk37/Cp,kpce,rho/blk38/d
      COMMON/blk39/dunit/blk40/l/blk41/Ce/blk43/lmd/blk44/Pjopt
      COMMON/blk45/qe/blk49/tauSRH/blk50/test1/blk53/Toff
      COMMON/blk54/c/blk55/V,w/blk56/A/blk57/tauAu/blk58/Ton
      COMMON/blk59/Ppceof,Ppceon,Rpceof,Rpceon,Vpceof,Vpceon
      COMMON/blk60/Rloadi/blk61/Ipcemx/blk62/Popt/blk63/q
      COMMON/blk70/CAu
      IF (d.GT.dunit) THEN
         Numdev = d/dunit
      ELSE
         Numdev = one
      ENDIF
      Rpceof = Vsrms/Ipceof
      Ppceof = Vsrms*Ipceof
      var1 = 1.5
      Nc = two*(((Mn*Mo/h)*(two*pi*k*Toff/h))**var1)
      Nv = two*(((Mp*Mo/h)*(two*pi*k*Toff/h))**var1)
      EgT = Ego-alpha*Toff*Toff/(Toff+beta)
      Ni = DSQRT(Nc*Nv)*DEXP(-EgT*q/(two*k*Toff))
      Po = (Na+DSQRT(Na*Na+two*two*Ni*Ni))/two
      No = Ni*Ni/Po
      Munoff = Mmne+(Mmxe-Mmne)/(one+(No/Nrfe)**alfe)
      Munon = Mmne+(Mmxe-Mmne)/(one+(Nmax/Nrfe)**alfe)
      Mupoff = Mmnh+(Mmxh-Mmnh)/(one+(Po/Nrfh)**alfh)
      Mupon = Mmnh+(Mmxh-Mmnh)/(one+(Nmax/Nrfh)**alfh)
      A = l/(Rpceof*q*(Munoff*No+Mupoff*Po))
      Rpceon = l/(q*A*(Munon+Mupon)*Nmax)
      Rload = Vsrms/Ipceon-Rs
```

```
      Rloadi = Rload
      Vpceon = Ipceon*Rpceon
      Ppceon = Vpceon*Ipceon
      tauAu = one/(CAu*Nmax*Nmax)
      tau = one/(one/tauSRH+one/tauAu)
      Popt = A*l*h*c*Nmax/(tau*lmd*qe)
      w = A/d
      V = A*l
      d = d/Numdev
      A = A/Numdev
      V = V/Numdev
      Rpceon = Rpceon*Numdev
      Ipceon = Ipceon/Numdev
      Ppceon = Ppceon/Numdev
      Popt = Popt/Numdev
      Pjopt = Pjopt/Numdev
      Pop = 0.0
      IF (INT(test1).EQ.1) Pop=Popt+Pjopt
      Rpceof = Rpceof*Numdev
      Ipceof = Ipceof/Numdev
      Vpceof = Vsrms
      Ppceof = Ppceof/Numdev
      Rtpce = d/(kpce*l*w*two)
      Ctpce = rho*V*Cp/two
      Ton = Tamb+(Popt+Ppceon)*Rtpce/two
      Toff = Tamb+Ppceof*Rtpce/two
      Temp = Tamb
      IF (INT(test1).EQ.1) Temp=Ton
      Vth = k*Ton/q
      La = DSQRT(two*Vth*Munon*Mupon*tau/(Munon+Mupon))
      Vsat = l*La/(Munon*tau)
      Ipcemx = Vsat/Rpceon
      Ipcemx = Ipcemx+Pjopt/Ce
      Vsat = Rpceon*Ipcemx
      WRITE (8,10) 0.0,0.0
      WRITE (8,10) Vsat,Ipcemx*Numdev
      WRITE (8,10) 1.3*Vsat,Ipcemx*Numdev
   10 FORMAT (1X,2(E14.7,1X))
      RETURN
      END
```

```
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine PSON1 calculates and outputs breaker parameters
C   during system on-state for the all-solid-state breaker:
C
      SUBROUTINE PSON1
      IMPLICIT DOUBLE PRECISION (A-Z)
      INTEGER convrg
      COMMON/blk02/Mun,Mup/blk03/No,Po/blk04/Nmax/blk05/one
      COMMON/blk06/t/blk09/ti/blk14/pi/blk15/Temp/blk16/two
      COMMON/blk17/Ctpce,Rtpce/blk18/Numdev/blk21/Ppce/blk22/dt
      COMMON/blk25/f/blk27/Rbr/blk30/Vsrms/blk31/Ibr
      COMMON/blk34/Con,phion/blk40/l/blk51/test2/blk52/tf/blk56/A
      COMMON/blk63/q/blk64/convrg/blk65/Ipce/blk66/Rpce,Vpce,Vs
      convrg = 0
      var1 = 150.0
      dt = (one/f)/var1
      var2 = Rtpce*Ctpce
      IF (var2.LT.dt) dt=var2
      IF (INT(test2).EQ.2.OR.INT(test2).EQ.4) THEN
         tend = tf
      ELSE
         tend = ti
      ENDIF
      GO TO 30
   10 WRITE (10,20) t, Vs, Ibr, Ipce, Vpce, Temp
   20 FORMAT (1X,E14.7,5(1X,E12.5))
      t = t+dt
      CALL PCETEM
   30 CALL EQCONC
      CALL MOBON
      Rpce = 1/(q*((Mun+Mup)*Nmax+Mup*Po+Mun*No)*A*Numdev)
      Rbr = Rpce
      CALL SSON
      Vs = DSQRT(two)*Vsrms*DSIN(two*pi*f*t)
      Ibr = Con*DSIN(two*pi*f*t-phion)
      Ipce = Ibr
      Vpce = Ipce*Rpce
      Ppce = Vpce*Ipce
      IF (DABS(Ipce).GT.1.0D+10) GO TO 40
      IF (Temp.GT.1000) GO TO 40
```

```
      IF (t.LT.tend) GO TO 10
      GO TO 50
   40 convrg = 1
   50 RETURN
      END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine PSON2 calculates and outputs breaker parameters
C   during system on-state for the hybrid breaker:
C
      SUBROUTINE PSON2
      IMPLICIT DOUBLE PRECISION (A-Z)
      INTEGER convrg
      COMMON/blk02/Mun,Mup/blk03/No,Po/blk05/one/blk06/t
      COMMON/blk07/to/blk14/pi/blk15/Temp/blk16/two
      COMMON/blk17/Ctpce,Rtpce/blk18/Numdev/blk21/Ppce/blk22/dt
      COMMON/blk25/f/blk27/Rbr/blk30/Vsrms/blk31/Ibr
      COMMON/blk34/Con,phion/blk40/l/blk47/Rmon/blk51/test2
      COMMON/blk52/tf/blk56/A/blk63/q/blk64/convrg/blk65/Ipce
      COMMON/blk66/Rpce,Vpce,Vs
      convrg = 0
      var1 = 150.0
      dt = (one/f)/var1
      var2 = Rtpce*Ctpce
      IF (var2.LT.dt) dt=var2
      IF (INT(test2).EQ.2.OR.INT(test2).EQ.4) THEN
         tend = tf
      ELSE
         tend = to
      ENDIF
      GO TO 30
   10 WRITE (10,20) t, Vs, Ibr, Ipce, Vpce, Temp
   20 FORMAT (1X,E14.7,5(1X,E12.5))
      t = t+dt
      CALL PCETEM
   30 CALL EQCONC
      CALL MOBOFF
      Rpce = l/(q*(Mup*Po+Mun*No)*A*Numdev)
      Rbr = one/(one/Rmon+one/Rpce)
      CALL SSON
      Vs = DSQRT(two)*Vsrms*DSIN(two*pi*f*t)
```

```
      Ibr = Con*DSIN(two*pi*f*t-phion)
      Ipce = Ibr*Rmon/(Rmon+Rpce)
      Vpce = Ipce*Rpce
      Ppce = Vpce*Ipce
      IF (DABS(Ipce).GT.1.0D+10) GO TO 40
      IF (Temp.GT.1000) GO TO 40
      IF (t.LT.tend) GO TO 10
      GO TO 50
   40 convrg = 1
   50 RETURN
      END
C*********************************************************************
C*********************************************************************
C*********************************************************************
C
C   Subroutine PSFLT1 calculates and outputs breaker parameters
C   during system fault-state for the all-solid-state breaker:
C
      SUBROUTINE PSFLT1
      IMPLICIT DOUBLE PRECISION (A-Z)
      INTEGER cntr,convrg,icntr
      COMMON/blk02/Mun,Mup/blk03/No,Po/blk04/Nmax/blk05/one
      COMMON/blk06/t/blk14/pi/blk15/Temp/blk16/two
      COMMON/blk17/Ctpce,Rtpce/blk18/Numdev/blk21/Ppce/blk22/dt
      COMMON/blk25/f/blk27/Rbr/blk28/Rload/blk29/Rs/blk30/Vsrms
      COMMON/blk31/Ibr/blk40/l/blk52/tf/blk56/A/blk61/Ipcemx
      COMMON/blk63/q/blk64/convrg/blk65/Ipce/blk66/Rpce,Vpce,Vs
      COMMON/blk67/Ipcetf,Vstf
      convrg = 0
      Vstf = Vs
      Ipcetf = Ipce
      tf = t
      Rload = 0.0
      var2 = 2.5
      var1 = DSQRT(two)*Vsrms/var2
      IF (Vs.LT.var1) THEN
         var1 = 4000.0
      ELSE
         var1 = 20000.0
      ENDIF
      dt = (one/f)/var1
      var3 = Rtpce*Ctpce
      IF (var3.LT.dt) dt=var3
```

```
      cntr = 0
      icntr = 0
      GO TO 20
   10 icntr = icntr+1
      IF (icntr.GT.cntr) icntr=0
      IF (icntr.NE.0) GO TO 40
   20 WRITE (10,30) t, Vs, Ibr, Ipce, Vpce, Temp
   30 FORMAT (1X,E14.7,5(1X,E12.5))
   40 CALL PCETEM
      CALL EQCONC
      CALL MOBON
      Rpce = 1/(q*((Mun+Mup)*Nmax+Mup*Po+Mun*No)*A*Numdev)
      Rbr = Rpce
      CALL SYSTM1
      Vs = DSQRT(two)*Vsrms*DSIN(two*pi*f*t)
      Ipce = Ibr
      IF (DABS(Ipce).GT.Ipcemx*Numdev) THEN
         Ipce = (DABS(Ipce)/Ipce)*Ipcemx*Numdev
         Ibr = Ipce
         Rtot = DABS(Vs)/DABS(Ibr)
         Rpce = Rtot-Rs-Rload
         Rbr = Rpce
         Vpce = Ipce*Rpce
         Ppce = Vpce*Ipce
         GO TO 60
      ENDIF
      Vpce = Ipce*Rpce
      Ppce = Vpce*Ipce
      IF (DABS(Ipce).GT.1.0D+10) GO TO 50
      IF (Temp.GT.1000) GO TO 50
      GO TO 10
   50 convrg = 1
   60 RETURN
      END
C*********************************************************************
C*********************************************************************
C*********************************************************************
C
C   Subroutine PSFLT2 calculates and outputs breaker parameters
C   during system fault-state for the hybrid breaker:
C
      SUBROUTINE PSFLT2
      IMPLICIT DOUBLE PRECISION (A-Z)
```

```
      INTEGER cntr,convrg,icntr
      COMMON/blk02/Mun,Mup/blk03/No,Po/blk05/one/blk06/t
      COMMON/blk07/to/blk14/pi/blk15/Temp/blk16/two
      COMMON/blk17/Ctpce,Rtpce/blk18/Numdev/blk21/Ppce/blk22/dt
      COMMON/blk25/f/blk27/Rbr/blk28/Rload/blk30/Vsrms/blk31/Ibr
      COMMON/blk33/Cflt,phiflt,tauflt/blk34/Con,phion/blk40/l
      COMMON/blk47/Rmon/blk52/tf/blk56/A/blk63/q/blk64/convrg
      COMMON/blk65/Ipce/blk66/Rpce,Vpce,Vs/blk67/Ipcetf,Vstf
      convrg = 0
      Vstf = Vs
      Ipcetf = Ipce
      tf = t
      tend = to
      Rload = 0.0
      var1 = 150.0
      dt = (one/f)/var1
      var2 = Rtpce*Ctpce
      IF (var2.LT.dt) dt=var2
      cntr = 3
      icntr = 0
      GO TO 20
   10 icntr = icntr+1
      IF (icntr.GT.cntr) icntr=0
      IF (icntr.NE.0) GO TO 40
   20 WRITE (10,30) t, Vs, Ibr, Ipce, Vpce, Temp
   30 FORMAT (1X,E14.7,5(1X,E12.5))
   40 t = t+dt
      CALL PCETEM
      CALL EQCONC
      CALL MOBOFF
      Rpce = l/(q*(Mup*Po+Mun*No)*A*Numdev)
      Rbr = one/(one/Rmon+one/Rpce)
      CALL SSFLT
      Vs = DSQRT(two)*Vsrms*DSIN(two*pi*f*t)
      Ibr = Cflt*DSIN(two*pi*f*t-phiflt)-
     $Cflt*DSIN(two*pi*f*tf-phiflt)*DEXP((tf-t)/tauflt)+
     $Con*DSIN(two*pi*f*tf-phion)*DEXP((tf-t)/tauflt)
      Ipce = Ibr*Rmon/(Rmon+Rpce)
      Vpce = Ipce*Rpce
      Ppce = Vpce*Ipce
      IF (DABS(Ipce).GT.1.0D+10) GO TO 50
      IF (Temp.GT.1000) GO TO 50
      IF (t.LT.tend) GO TO 10
```

```
      GO TO 60
   50 convrg = 1
   60 RETURN
      END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine PSINT1 calculates and outputs breaker parameters
C   during system interrupt-state for the all-solid-state
C   breaker:
C
      SUBROUTINE PSINT1
      IMPLICIT DOUBLE PRECISION (A-Z)
      INTEGER cntr,convrg,icntr
      COMMON/blk02/Mun,Mup/blk03/No,Po/blk04/Nmax/blk05/one
      COMMON/blk06/t/blk08/tau/blk09/ti/blk14/pi/blk15/Temp
      COMMON/blk16/two/blk18/Numdev/blk20/Pop/blk21/Ppce/blk22/dt
      COMMON/blk25/f/blk26/Ls/blk27/Rbr/blk28/Rload/blk29/Rs
      COMMON/blk30/Vsrms/blk31/Ibr/blk40/l/blk42/delint/blk56/A
      COMMON/blk61/Ipcemx/blk63/q/blk64/convrg/blk65/Ipce
      COMMON/blk66/Rpce,Vpce,Vs/blk68/Ipceti,Vsti,tendi,dtint
      convrg = 0
      Vsti = Vs
      Ipceti = Ipce
      ti = t
      Pop = 0.0
      tend = ti+delint
      var4 = 200.0
      var5 = (tend-ti)/var4
      dt = two*Ls/(Rbr+Rload+Rs)
      IF (var5.LT.dt) THEN
         dt = var5
         cntr = 0
      ELSE
         var6 = ((tend-ti)/dt)/var4
         cntr = INT(var6)
      ENDIF
      icntr = 0
      GO TO 20
   10 icntr = icntr+1
      IF (icntr.GT.cntr) icntr=0
      IF (icntr.NE.0) GO TO 40
```

```
 20 WRITE (10,30) t, Vs, Ibr, Ipce, Vpce, Temp
 30 FORMAT (1X,E14.7,5(1X,E12.5))
 40 CALL PCETEM
    CALL EQCONC
    CALL SYSTM1
    CALL MOBINT
    var1 = 1/(q*((Mun+Mup)*Nmax*DEXP((ti-t)/tau)+Mup*Po+
   $Mun*No)*A*Numdev)
    IF (var1.GE.Rpce) Rpce=var1
    Rbr = Rpce
    Vs = DSQRT(two)*Vsrms*DSIN(two*pi*f*t)
    Ipce = Ibr
    Vpce = Ipce*Rpce
    var2 = 1.5
    var3 = var2*DSQRT(two)*Vsrms
    IF (DABS(Vpce).GT.var3) THEN
       Vpce = var3*(Vpce/DABS(Vpce))
       Ipce = Vpce/Rpce
    ENDIF
    IF (Rpce.GT.var1) THEN
       Ipce = (DABS(Ipce)/Ipce)*Ipcemx*Numdev
       Ibr = Ipce
       Rtot = DABS(Vs)/DABS(Ibr)
       Rpce = Rtot-Rs-Rload
       Rbr = Rpce
       Vpce = Ipce*Rpce
    ENDIF
    Ppce = Vpce*Ipce
    dt = two*Ls/(Rbr+Rload+Rs)
    IF (var5.LT.dt) THEN
       dt = var5
       cntr = 0
    ELSE
       var6 = ((tend-ti)/dt)/var4
       cntr = INT(var6)
    ENDIF
    IF (DABS(Ipce).GT.1.0D+10) GO TO 50
    IF (Temp.GT.1000) GO TO 50
    IF (t.LT.tend) GO TO 10
    GO TO 60
 50 convrg = 1
 60 tendi = t
    dtint = tendi-ti
```

```
      RETURN
      END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine PSINT2 calculates and outputs breaker parameters
C   during system interrupt-state for the hybrid breaker:
C
      SUBROUTINE PSINT2
      IMPLICIT DOUBLE PRECISION (A-Z)
      INTEGER cntr,convrg,icntr
      COMMON/blk02/Mun,Mup/blk03/No,Po/blk04/Nmax/blk05/one
      COMMON/blk06/t/blk07/to/blk08/tau/blk09/ti/blk14/pi
      COMMON/blk15/Temp/blk16/two/blk18/Numdev/blk20/Pop
      COMMON/blk21/Ppce/blk22/dt/blk25/f/blk26/Ls/blk27/Rbr
      COMMON/blk28/Rload/blk29/Rs/blk30/Vsrms/blk31/Ibr/blk40/I
      COMMON/blk42/delint/blk44/Pjopt/blk46/Rmof/blk47/Rmon
      COMMON/blk48/taum/blk56/A/blk61/Ipcemx/blk62/Popt/blk63/q
      COMMON/blk64/convrg/blk65/Ipce/blk66/Rpce,Vpce,Vs
      COMMON/blk68/Ipceti,Vsti,tendi,dtint/blk69/Ipceto,Vsto
      convrg = 0
      undrfl = 200.0
      Vsto = Vs
      Ipceto = Ipce
      to = t
      Pop = Popt+Pjopt
      tend = ti
      var4 = 150.0
      var5 = (tend-to)/var4
      dt = two*Ls/(Rbr+Rload+Rs)
      IF (var5.LT.dt) THEN
         dt = var5
         cntr = 0
      ELSE
         var6 = ((tend-to)/dt)/var4
         cntr = INT(var6)
      ENDIF
      icntr = 0
      GO TO 20
   10 icntr = icntr+1
      IF (icntr.GT.cntr) icntr=0
      IF (icntr.NE.0) GO TO 40
```

```
20 WRITE (10,30) t, Vs, Ibr, Ipce, Vpce, Temp
30 FORMAT (1X,E14.7,5(1X,E12.5))
40 CALL PCETEM
   CALL EQCONC
   CALL SYSTM1
   IF ((t-to)/tau.GT.undrfl) GO TO 50
   CALL MOBTON
   Rpce = 1/(q*((Mun+Mup)*Nmax*(one-DEXP((to-t)/tau))+Mup*Po+
  $Mun*No)*A*Numdev)
   GO TO 60
50 CALL MOBON
   Rpce = 1/(q*((Mun+Mup)*Nmax+Mup*Po+Mun*No)*A*Numdev)
60 Rm = Rmon+Rmof*(one-DEXP((to-t)/taum))
   Rbr = one/(one/Rm+one/Rpce)
   Vs = DSQRT(two)*Vsrms*DSIN(two*pi*f*t)
   Ipce = Ibr*Rm/(Rm+Rpce)
   Vpce = Ipce*Rpce
   Ppce = Vpce*Ipce
   dt = two*Ls/(Rbr+Rload+Rs)
   IF (var5.LT.dt) THEN
      dt = var5
      cntr = 0
   ELSE
      var6 = ((tend-to)/dt)/var4
      cntr = INT(var6)
   ENDIF
   IF (DABS(Ipce).GT.1.0D+10) GO TO 150
   IF (Temp.GT.1000) GO TO 150
   IF (t.LT.tend) GO TO 10
   Vsti = Vs
   Ipceti = Ipce
   ti = t
   Pop = 0.0
   tend = ti+delint
   var4 = 200.0
   var5 = (tend-ti)/var4
   dt = two*Ls/(Rbr+Rload+Rs)
   IF (var5.LT.dt) THEN
      dt = var5
      cntr = 0
   ELSE
      var6 = ((tend-ti)/dt)/var4
      cntr = INT(var6)
```

```
      ENDIF
      icntr = 0
      GO TO 120
  110 icntr = icntr+1
      IF (icntr.GT.cntr) icntr=0
      IF (icntr.NE.0) GO TO 140
  120 WRITE (10,130) t, Vs, Ibr, Ipce, Vpce, Temp
  130 FORMAT (1X,E14.7,5(1X,E12.5))
  140 CALL PCETEM
      CALL EQCONC
      CALL SYSTM1
      CALL MOBINT
      Rpce = 1/(q*((Mun+Mup)*Nmax*DEXP((ti-t)/tau)+Mup*Po+
     $Mun*No)*A*Numdev)
      Rbr = one/(one/Rmof+one/Rpce)
      Vs = DSQRT(two)*Vsrms*DSIN(two*pi*f*t)
      Ipce = Ibr*Rmof/(Rmof+Rpce)
      Vpce = Ipce*Rpce
      var2 = 1.5
      var3 = var2*DSQRT(two)*Vsrms
      IF (DABS(Vpce).GT.var3) THEN
         Vpce = var3*(Vpce/DABS(Vpce))
         Ipce = Vpce/Rpce
      ENDIF
      Ppce = Vpce*Ipce
      dt = two*Ls/(Rbr+Rload+Rs)
      IF (var5.LT.dt) THEN
         dt = var5
         cntr = 0
      ELSE
         var6 = ((tend-ti)/dt)/var4
         cntr = INT(var6)
      ENDIF
      IF (DABS(Ipce).GT.1.0D+10) GO TO 150
      IF (Temp.GT.1000) GO TO 150
      IF (t.LT.tend) GO TO 110
      GO TO 160
  150 convrg = 1
  160 tendi = t
      dtint = tendi-ti
      RETURN
      END
```

```
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine SSON calculates various system on-constants:
C
      SUBROUTINE SSON
      IMPLICIT DOUBLE PRECISION (A-Z)
      COMMON/blk14/pi/blk16/two/blk25/f/blk26/Ls/blk27/Rbr
      COMMON/blk28/Rload/blk29/Rs/blk30/Vsrms/blk34/Con,phion
      var1 = Rs+Rbr+Rload
      var2 = two*pi*f*Ls
      var3 = var2/var1
      phion = DATAN(var3)
      var1 = var1*var1
      var2 = var2*var2
      var3 = var1+var2
      var3 = DSQRT(var3)
      Con = DSQRT(two)*Vsrms/var3
      RETURN
      END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine SSFLT calculates various system fault-constants:
C
      SUBROUTINE SSFLT
      IMPLICIT DOUBLE PRECISION (A-Z)
      COMMON/blk14/pi/blk16/two/blk25/f/blk26/Ls/blk27/Rbr
      COMMON/blk28/Rload/blk29/Rs/blk30/Vsrms
      COMMON/blk33/Cflt,phiflt,tauflt
      var1 = Rs+Rbr+Rload
      var2 = two*pi*f*Ls
      var3 = var2/var1
      phiflt = DATAN(var3)
      var1 = var1*var1
      var2 = var2*var2
      var3 = var1+var2
      var3 = DSQRT(var3)
      Cflt = DSQRT(two)*Vsrms/var3
      tauflt = Ls/(Rs+Rbr+Rload)
      RETURN
      END
```

```
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine SYSTM1 calculates the system current during a
C   transient:
C
      SUBROUTINE SYSTM1
      IMPLICIT DOUBLE PRECISION (A-Z)
      INTEGER I
      DIMENSION F1(3),F2(3),F3(3),F4(3),X(3),Y(3)
      COMMON/blk06/t/blk16/two/blk22/dt/blk23/six/blk31/Ibr
      X(1) = t
      X(2) = Ibr
      CALL FX1 (F1,X)
      DO 10 I=1, 2
   10 Y(I) = X(I)+dt*F1(I)/two
      CALL FX1 (F2,Y)
      DO 20 I=1, 2
   20 Y(I) = X(I)+dt*F2(I)/two
      CALL FX1 (F3,Y)
      DO 30 I=1, 2
   30 Y(I) = X(I)+dt*F3(I)
      CALL FX1 (F4,Y)
      DO 40 I=1, 2
   40 X(I) = X(I)+dt*(F1(I)+two*(F2(I)+F3(I))+F4(I))/six
      t = X(1)
      Ibr = X(2)
      RETURN
      END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine FX1 defines the system differential equations:
C
      SUBROUTINE FX1 (FUN,X)
      IMPLICIT DOUBLE PRECISION (A-Z)
      DIMENSION FUN(3),X(3)
      COMMON/blk05/one/blk14/pi/blk16/two/blk25/f/blk26/Ls
      COMMON/blk27/Rbr/blk28/Rload/blk29/Rs/blk30/Vsrms
      FUN(1) = one
      FUN(2) = -(Rbr+Rs+Rload)*X(2)/Ls+DSQRT(two)*Vsrms*
```

```
      $DSIN(two*pi*f*X(1))/Ls
       RETURN
       END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine PCETEM calculates the temperature of the PCE
C   during its operation:
C
       SUBROUTINE PCETEM
       IMPLICIT DOUBLE PRECISION (A-Z)
       INTEGER I
       DIMENSION Ge1(2),Ge2(2),Ge3(2),Ge4(2),X1(2),Y1(2)
       COMMON/blk15/Temp/blk16/two/blk22/dt/blk23/six
       X1(1) = Temp
       CALL FX2 (Ge1,X1)
       DO 10 I=1, 1
    10 Y1(I) = X1(I)+dt*Ge1(I)/two
       CALL FX2 (Ge2,Y1)
       DO 20 I=1, 1
    20 Y1(I) = X1(I)+dt*Ge2(I)/two
       CALL FX2 (Ge3,Y1)
       DO 30 I=1, 1
    30 Y1(I) = X1(I)+dt*Ge3(I)
       CALL FX2 (Ge4,Y1)
       DO 40 I=1, 1
    40 X1(I) = X1(I)+dt*(Ge1(I)+two*(Ge2(I)+Ge3(I))+Ge4(I))/six
       Temp = X1(1)
       RETURN
       END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine FX2 defines the thermal differential equations:
C
       SUBROUTINE FX2 (FUN1,X1)
       IMPLICIT DOUBLE PRECISION (A-Z)
       DIMENSION FUN1(2),X1(2)
       COMMON/blk16/two/blk17/Ctpce,Rtpce/blk18/Numdev/blk19/Tamb
       COMMON/blk20/Pop/blk21/Ppce
       FUN1(1) = ((Tamb-X1(1))/Rtpce+Ppce/(two*Numdev)+Pop/two)/
```

```
      $Ctpce
       RETURN
       END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine EQCONC calculates the equilibrium concentration
C   of No and Po:
C
       SUBROUTINE EQCONC
       IMPLICIT DOUBLE PRECISION (A-Z)
       COMMON/blk03/No,Po/blk10/alpha,beta,Ego/blk11/Mn,Mp
       COMMON/blk12/h,k/blk13/Na/blk14/pi/blk15/Temp/blk16/two
       COMMON/blk35/Mo/blk63/q
       var1 = 1.5
       Nc = two*(((Mn*Mo/h)*(two*pi*k*Temp/h))**var1)
       Nv = two*(((Mp*Mo/h)*(two*pi*k*Temp/h))**var1)
       EgT = Ego-alpha*Temp*Temp/(Temp+beta)
       Ni = DSQRT(Nc*Nv)*DEXP(-EgT*q/(two*k*Temp))
       Po = (Na+DSQRT(Na*Na+two*two*Ni*Ni))/two
       No = Ni*Ni/Po
       RETURN
       END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine MOBON calculates the electron and hole mobilities
C   during the PCE on-state:
C
       SUBROUTINE MOBON
       IMPLICIT DOUBLE PRECISION (A-Z)
       COMMON/blk01/Mmxe,Mmne,Nrfe,alfe,Mmxh,Mmnh,Nrfh,alfh
       COMMON/blk02/Mun,Mup/blk03/No,Po/blk04/Nmax/blk05/one
       Mun = Mmne+(Mmxe-Mmne)/(one+((No+Nmax)/Nrfe)**alfe)
       Mup = Mmnh+(Mmxh-Mmnh)/(one+((Po+Nmax)/Nrfh)**alfh)
       RETURN
       END
C*****************************************************************
C*****************************************************************
C*****************************************************************
```

```
C
C   Subroutine MOBTON calculates the electron and hole mobilities
C   during the PCE turn-on-state:
C
      SUBROUTINE MOBTON
      IMPLICIT DOUBLE PRECISION (A-Z)
      COMMON/blk01/Mmxe,Mmne,Nrfe,alfe,Mmxh,Mmnh,Nrfh,alfh
      COMMON/blk02/Mun,Mup/blk03/No,Po/blk04/Nmax/blk05/one
      COMMON/blk06/t/blk07/to/blk08/tau
      Mun = Mmne+(Mmxe-Mmne)/(one+((Nmax*(one-DEXP((to-t)/tau))
     $+No)/Nrfe)**alfe)
      Mup = Mmnh+(Mmxh-Mmnh)/(one+((Nmax*(one-DEXP((to-t)/tau))
     $+Po)/Nrfh)**alfh)
      RETURN
      END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine MOBINT calculates the electron and hole mobilities
C   during the PCE interruption-state:
C
      SUBROUTINE MOBINT
      IMPLICIT DOUBLE PRECISION (A-Z)
      COMMON/blk01/Mmxe,Mmne,Nrfe,alfe,Mmxh,Mmnh,Nrfh,alfh
      COMMON/blk02/Mun,Mup/blk03/No,Po/blk04/Nmax/blk05/one
      COMMON/blk06/t/blk08/tau/blk09/ti
      Mun = Mmne+(Mmxe-Mmne)/(one+((Nmax*DEXP((ti-t)/tau)+No)
     $/Nrfe)**alfe)
      Mup = Mmnh+(Mmxh-Mmnh)/(one+((Nmax*DEXP((ti-t)/tau)+Po)
     $/Nrfh)**alfh)
      RETURN
      END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine MOBOFF calculates the electron and hole mobilities
C   during the PCE off-state:
C
      SUBROUTINE MOBOFF
```

```
      IMPLICIT DOUBLE PRECISION (A-Z)
      COMMON/blk01/Mmxe,Mmne,Nrfe,alfe,Mmxh,Mmnh,Nrfh,alfh
      COMMON/blk02/Mun,Mup/blk03/No,Po/blk05/one
      Mun = Mmne+(Mmxe-Mmne)/(one+(No/Nrfe)**alfe)
      Mup = Mmnh+(Mmxh-Mmnh)/(one+(Po/Nrfh)**alfh)
      RETURN
      END
C*****************************************************************
C*****************************************************************
C*****************************************************************
C
C   Subroutine PCEDEV is used to output given and calculated
C   information regarding the PCE:
C
      SUBROUTINE PCEDEV
      IMPLICIT DOUBLE PRECISION (A-Z)
      COMMON/blk04/Nmax/blk07/to/blk08/tau/blk09/ti/blk13/Na
      COMMON/blk15/Temp/blk17/Ctpce,Rtpce/blk18/Numdev/blk19/Tamb
      COMMON/blk26/Ls/blk29/Rs/blk36/Ipceof,Ipceon/blk38/d
      COMMON/blk40/l/blk44/Pjopt/blk49/tauSRH/blk50/test1
      COMMON/blk51/test2/blk52/tf/blk53/Toff/blk55/V,w/blk56/A
      COMMON/blk57/tauAu/blk58/Ton
      COMMON/blk59/Ppceof,Ppceon,Rpceof,Rpceon,Vpceof,Vpceon
      COMMON/blk60/Rloadi/blk61/Ipcemx/blk62/Popt/blk65/Ipce
      COMMON/blk67/Ipcetf,Vstf/blk68/Ipceti,Vsti,tendi,dtint
      COMMON/blk69/Ipceto,Vsto
C
C   Output the number of parallel devices to be used:
C
      WRITE (6,10) INT(Numdev)
   10 FORMAT (1X,'NUMBER OF PCE DEVICES IN PARALLEL:',1X,I4)
C
C   Output the given device parameters:
C
      WRITE (6,20)
   20 FORMAT (/1X,'GIVEN DEVICE PARAMETERS:')
      WRITE (6,21) Na
   21 FORMAT (15X,'Na :',1X,E10.3,1X,'m-cu inv.')
      WRITE (6,22) Nmax
   22 FORMAT (15X,'Nmax :',1X,E10.3,1X,'m-cu inv.')
      WRITE (6,23) tauAu
   23 FORMAT (15X,'tauAu :',1X,E10.3,1X,'sec')
      WRITE (6,24) tauSRH
```

```
   24 FORMAT (15X,'tauSRH:',1X,E10.3,1X,'sec')
      WRITE (6,25) tau
   25 FORMAT (15X,'tau :',1X,E10.3,1X,'sec')
C
C    Output the calculated device dimensions:
C
      WRITE (6,30)
   30 FORMAT (/1X,'DEVICE DIMENSIONS:',28X,'TOTAL')
      WRITE (6,31) l,l
   31 FORMAT (15X,'l :',1X,E10.3,1X,'m',9X,E10.3)
      WRITE (6,32) d,d*Numdev
   32 FORMAT (15X,'d :',1X,E10.3,1X,'m',9X,E10.3)
      WRITE (6,33) w,w
   33 FORMAT (15X,'w :',1X,E10.3,1X,'m',9X,E10.3)
      WRITE (6,34) A,A*Numdev
   34 FORMAT (15X,'A :',1X,E10.3,1X,'m-sq',6X,E10.3)
      WRITE (6,35) V,V*Numdev
   35 FORMAT (15X,'V :',1X,E10.3,1X,'m-cu',6X,E10.3)
C
C    Output the calculated steady-state-on conditions:
C
      WRITE (6,40)
   40 FORMAT (/1X,'DEVICE ON-CONDITIONS:')
      WRITE (6,41) Rpceon,Rpceon/Numdev
   41 FORMAT (15X,'Rpceon:',1X,E10.3,1X,'ohms',6X,E10.3)
      WRITE (6,42) Vpceon,Vpceon
   42 FORMAT (15X,'Vpceon:',1X,E10.3,1X,'Vrms',6X,E10.3)
      WRITE (6,43) Ipceon,Ipceon*Numdev
   43 FORMAT (15X,'Ipceon:',1X,E10.3,1X,'Arms',6X,E10.3)
      WRITE (6,44) Ipcemx,Ipcemx*Numdev
   44 FORMAT (15X,'Ipcemx:',1X,E10.3,1X,'Amps',6X,E10.3)
      WRITE (6,45) Ppceon,Ppceon*Numdev
   45 FORMAT (15X,'Ppceon:',1X,E10.3,1X,'watts',5X,E10.3)
      WRITE (6,46) Popt,Popt*Numdev
   46 FORMAT (15X,'Popt :',1X,E10.3,1X,'watts',5X,E10.3)
      WRITE (6,47) Pjopt,Pjopt*Numdev
   47 FORMAT (15X,'Pjopt :',1X,E10.3,1X,'watts',5X,E10.3)
C
C    Output the calculated steady-state-off conditions:
C
      WRITE (6,50)
   50 FORMAT (/1X,'DEVICE OFF-CONDITIONS:')
      WRITE (6,51) Rpceof,Rpceof/Numdev
```

```
   51 FORMAT (15X,'Rpceof:',1X,E10.3,1X,'ohms',6X,E10.3)
      WRITE (6,52) Vpceof,Vpceof
   52 FORMAT (15X,'Vpceof:',1X,E10.3,1X,'Vrms',6X,E10.3)
      WRITE (6,53) Ipceof,Ipceof*Numdev
   53 FORMAT (15X,'Ipceof:',1X,E10.3,1X,'Arms',6X,E10.3)
      WRITE (6,54) Ppceof,Ppceof*Numdev
   54 FORMAT (15X,'Ppceof:',1X,E10.3,1X,'watts',5X,E10.3)
C
C   Output the thermal parameters:
C
      WRITE (6,60)
   60 FORMAT (/1X,'THERMAL PARAMETERS:')
      WRITE (6,61) Rtpce
   61 FORMAT (15X,'Rtpce :',1X,E10.3,1X,'K/W')
      WRITE (6,62) Ctpce
   62 FORMAT (15X,'Ctpce :',1X,E10.3,1X,'W.sec/K')
      WRITE (6,63) Tamb
   63 FORMAT (15X,'Tamb :',1X,E10.3,1X,'K')
      WRITE (6,64) Ton
   64 FORMAT (15X,'Ton :',1X,E10.3,1X,'K')
      WRITE (6,65) Toff
   65 FORMAT (15X,'Toff :',1X,E10.3,1X,'K')
C
C   Output the system parameters:
C
      WRITE (6,70)
   70 FORMAT (/1X,'SYSTEM PARAMETERS:')
      WRITE (6,71) Ls
   71 FORMAT (15X,'Ls :',1X,E10.3,1X,'H')
      WRITE (6,72) Rs
   72 FORMAT (15X,'Rs :',1X,E10.3,1X,'ohms')
      WRITE (6,73) Rloadi
   73 FORMAT (15X,'Rload :',1X,E10.3,1X,'ohms')
C
C   Output the operating conditions:
C
  100 IF (INT(test2).NE.2.AND.INT(test2).NE.3.AND.
     $INT(test2).NE.4) GO TO 400
      WRITE (6,80)
   80 FORMAT (/1X,'OPERATING CONDITIONS:')
      IF (INT(test2).NE.2.AND.INT(test2).NE.4) GO TO 200
      WRITE (6,81) Vstf
   81 FORMAT (15X,'Vstf :',1X,E13.6,1X,'V')
```

```
      WRITE (6,82) Ipcetf
   82 FORMAT (15X,'Ipcetf:',1X,E13.6,1X,'A')
      WRITE (6,83) tf
   83 FORMAT (15X,'tf :',1X,E13.6,1X,'sec')
  200 IF (INT(test2).NE.3.AND.INT(test2).NE.4) GO TO 400
      IF (INT(test1).EQ.1) GO TO 300
      WRITE (6,84) Vsto
   84 FORMAT (15X,'Vsto :',1X,E13.6,1X,'V')
      WRITE (6,85) Ipceto
   85 FORMAT (15X,'Ipceto:',1X,E13.6,1X,'A')
      WRITE (6,86) to
   86 FORMAT (15X,'to :',1X,E13.6,1X,'sec')
  300 WRITE (6,88) Vsti
   88 FORMAT (15X,'Vsti :',1X,E13.6,1X,'V')
      WRITE (6,89) Ipceti
   89 FORMAT (15X,'Ipceti:',1X,E13.6,1X,'A')
      WRITE (6,90) ti
   90 FORMAT (15X,'ti :',1X,E13.6,1X,'sec')
      WRITE (6,91) tendi
   91 FORMAT (15X,'tendi :',1X,E13.6,1X,'sec')
      WRITE (6,92) dtint
   92 FORMAT (15X,'dtint :',1X,E13.6,1X,'sec')
  400 IF (INT(test2).EQ.1) GO TO 500
      IF (ABS(Ipce).GT.1.0D+10) GO TO 600
  500 IF (Temp.LE.1000) GO TO 900
  600 DO 700 I=1, 3
  700 WRITE (6,800)
  800 FORMAT (//1X,'Sorry !!!  PCE blown-up !!!')
  900 RETURN
      END
C*********************************************************************
C*********************************************************************
C*********************************************************************
```

REFERENCES

[1] B. Y. Hwang, F. A. Lindholm, and R. B. Hammond, "Methodology for Calculating Turn-Off Transients of Photoconductive Circuit Elements in Picosecond Optoelectronics," IEEE Journal of Quantum Electronics, Vol. QE-19, No. 4, April 1983, pp. 648–657.

[2] C. P. Triaros, D. P. Carroll, and F. A. Lindholm, "Photoconductive Switches for AC Circuit Protection," IEEE Transactions on Electron Devices, Vol. 37, No. 12, Dec. 1990, pp. 2526–2531.

[3] D. H. Auston, "Picosecond Optoelectronic Switching and Gating in Silicon," Applied Physics Letters, Vol. 26, No. 3, Feb. 1975, pp. 101–103.

[4] W. C. Nunnally and R. B. Hammond, "80–MW Photoconductor Power Switch," Applied Physics Letters, Vol. 44, Feb. 1984, pp. 980–982.

[5] R. A. Petr, W. C. Nunnally, and C. V. Smith, "Cryogenic Silicon Photoconductive Switches for High Power Lasers," SPIE Proceedings, Vol. 871, Jan. 1988, pp. 297–306.

[6] P. A. Basore, D. T. Rover, and A.W. Smith, "PC-1D Version 2: Enhanced Numerical Solar Cell Modeling," 20th IEEE Photovoltaic Specialists Conf., Las Vegas, Sept. 1988.

[7] L. C. Roberts, "The Fabrication and Testing of Silicon Photoconductive Circuit Elements for Power System Applications," Thesis, University of Florida, 1990.

[8] A. E. Iverson, "The Mathematical Modeling of Photoconductive Power Switches," Transactions of the Society for Computer Simulation, Vol. 5, No. 3, July 1988, pp. 175–191.

[9] S. E. Thompson and F. A. Lindholm, "Influence of Heavily Doped Contacts on Photoconductive Switch Properties," IEEE Transactions on Electron Devices, Vol. 37, No. 12, Dec. 1990, pp. 2542–2553.

[10] S. M. Sze, Physics of Semiconductor Devices, Second ed., Wiley-Interscience, New York, 1981.

[11] F. J. Zutavern, G. M. Loubriel, M. W. O'Malley, L. P. Shanwald, W. D. Helgerson, D. L. McLaughlin, and B. B. McKenzie, "Photoconductive Semiconductor Switch Experiments for Pulsed Power Applications," IEEE Transactions on Electron Devices, Vol. 37, No. 12, Dec. 1990, pp. 2472–2477.

[12] B. G. Streetman, Solid State Electronic Devices, Second ed., Prentice Hall, Englewood Cliffs, New Jersey, 1980.

[13] C. D. Thurmond, "The Standard Thermodynamic Functions for the Formation of Electrons and Holes in Ge, Si, GaAs, and GaP," Journal of Electrochemical Society, Vol. 122, No. 8, Aug. 1975, pp. 1133–1141.

[14] D. M. Caughey and R. E. Thomas, "Carrier Mobilities in Silicon Empirically Related to Doping and Field," Proceedings of the IEEE, Dec. 1967, pp. 2192–2193.

[15] K. Misiakos, Ju-Sung Park, and A. Neugroschel, "Carrier Lifetimes in Highly Injected Silicon," Journal of Applied Physics, Vol. 67, No. 5, March 1990, pp. 2576–2582.

[16] J. H. Seely and R. C. Chu, Heat Transfer in Microelectronic Equipment, M. Dekker, New York, 1972.

[17] F. Kreith and W. Black, Basic Heat Transfer, Harper & Row, New York, 1980.

[18] A. H. Iversen and S. Whitaker, "A Uniform Temperature, Ultra High Heat Flux Liquid Cooled, Power Semi-Conductor Package," IAS-IEEE Annual Meeting, San Diego, Oct. 1989.

[19] H. D. Barber, "Effective Mass and Intrinsic Concentration in Silicon," Solid State Electronics, Vol. 10, No. 11, Nov. 1967, pp. 1039–1051.

[20] G. D. Pitt and J. Lees, "The X_{1c} Conduction Band Minimum in High Purity Epitaxial n-Type Gallium Arsenide," Solid State Communications, Vol. 8, No. 7, April 1970, pp. 419–495.

[21] O. V. Emelyanenko, "Dependence of the Thermal EMF on the Hole Generation in Gallium Arsenide Crystals, Phys. Status Solidi, Vol. 8, No. 3, March 1965, pp. K155–K158.

[22] R. A. Sinton and R. M. Swanson, "Recombination in Highly Injected Silicon," IEEE Transactions on Electron Devices, Vol. ED-34, No. 6, June 1987, pp. 1380–1389.

[23] P. T. Landsberg, "The Band-Band Auger Effect in Semiconductors," Solid State Electronics, Vol. 30, No. 11, Nov. 1987, pp. 1107–1115.

BIOGRAPHICAL SKETCH

Christos P. Triaros was born in Famagusta, Cyprus, on December 25, 1961. He received the B.S.E.E. and M.E. in electrical engineering degrees from the University of Florida, Gainesville, in 1986 and 1988, respectively. He is currently working toward the Ph.D. degree in electrical engineering at the University of Florida, which he expects to receive in May of 1991. His research involves a study to investigate the feasibility of photoconductive switches for protective switching applications in AC power transmission and distribution circuits.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Dennis P. Carroll, Chairman
Professor of Electrical Engineering

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Gys Bosman
Professor of Electrical Engineering

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Alexander Domijan, Jr.
Assistant Professor of Electrical Engineering

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Fred A. Lindholm
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

A. Neugroschel

Arnost Neugroschel
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Arun Kumar Varma

Arun K. Varma
Professor of Mathematics

This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

May 1991

for Winfred M. Phillips
Dean, College of Engineering

Madelyn M. Lockhart
Dean, Graduate School